Signetics

FAST Products

FAST 74F5074 FLIP-FLOP

Synchronizing Dual D-Type Flip-Flop With Metastable Immune Charateristics

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	200 MHz	18mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **Same pinout and function as 74F74**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F5074N
14-Pin Plastic SO	N74F5074D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

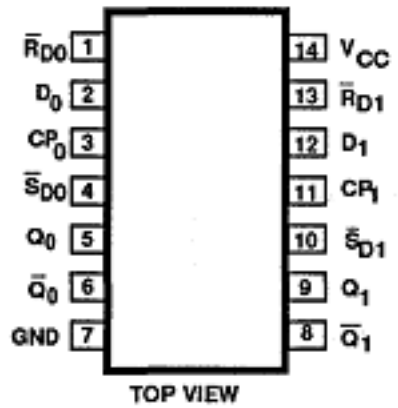
The 74F5074 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

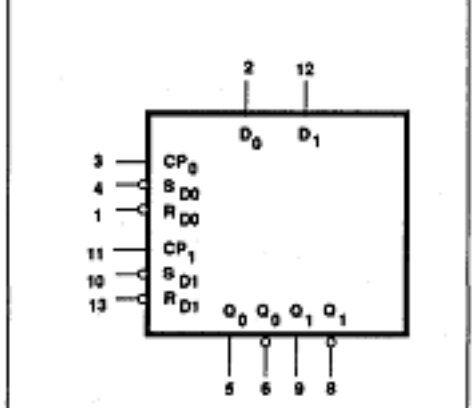
Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold times violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: τ < .200ns, T_0=10 µs, and h=3.8ns.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)