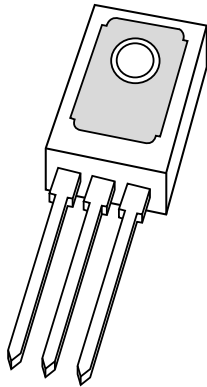


DATA SHEET



BD132 PNP power transistor

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC04

1997 Mar 04

PNP power transistor

BD132

FEATURES

- High current (max. 3 A)
- Low voltage (max. 45 V).

APPLICATIONS

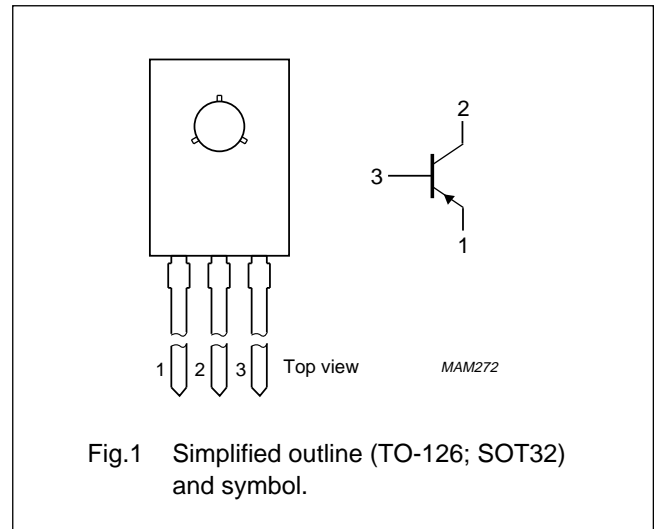
- General purpose power applications.

DESCRIPTION

PNP power transistor in a TO-126; SOT32 plastic package. NPN complement: BD131.

PINNING

PIN	DESCRIPTION
1	emitter
2	collector, connected to metal part of mounting surface
3	base



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–45	V
V_{CEO}	collector-emitter voltage	open base	–	–45	V
I_{CM}	peak collector current		–	–6	A
P_{tot}	total power dissipation	$T_{mb} \leq 60\text{ }^\circ\text{C}$	–	15	W
h_{FE}	DC current gain	$I_C = -0.5\text{ A}; V_{CE} = -12\text{ V}$	40	–	
f_T	transition frequency	$I_C = -0.25\text{ A}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}$	60	–	MHz

PNP power transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–45	V
V_{CEO}	collector-emitter voltage	open base	–	–45	V
V_{EBO}	emitter-base voltage	open collector	–	–4	V
I_C	collector current (DC)		–	–3	A
I_{CM}	peak collector current		–	–6	A
I_{BM}	peak base current		–	–0.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 60\text{ °C}$	–	15	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	100	K/W
$R_{th\ j-mb}$	thermal resistance from junction to mounting base		6	K/W

Note

1. Refer to TO-126; SOT32 standard mounting conditions.

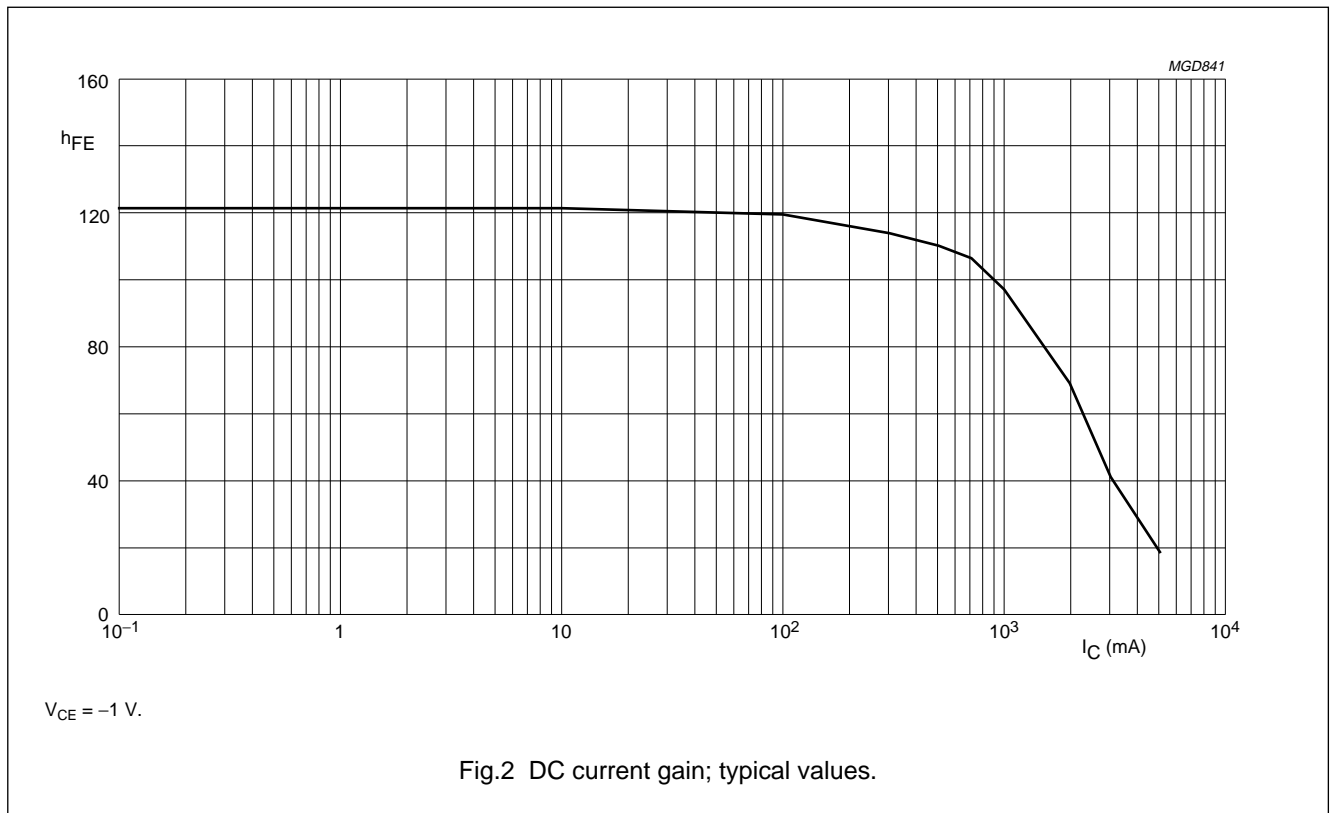
PNP power transistor

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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = -40\text{ V}$	–	–50	nA
		$I_E = 0; V_{CB} = -40\text{ V}; T_j = 150\text{ }^\circ\text{C}$	–	–10	μA
I_{EBO}	emitter cut-off current	$I_C = 0; V_{EB} = -3\text{ V}$	–	–50	nA
h_{FE}	DC current gain	$I_C = -0.5\text{ A}; V_{CE} = -12\text{ V}$	40	–	
		$I_C = -2\text{ A}; V_{CE} = -1\text{ V}$; see Fig.2	20	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	–	–300	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–700	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	–	–1.2	V
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	–	–1.5	V
f_T	transition frequency	$I_C = -0.25\text{ A}; V_{CE} = -5\text{ V}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}$	60	–	MHz

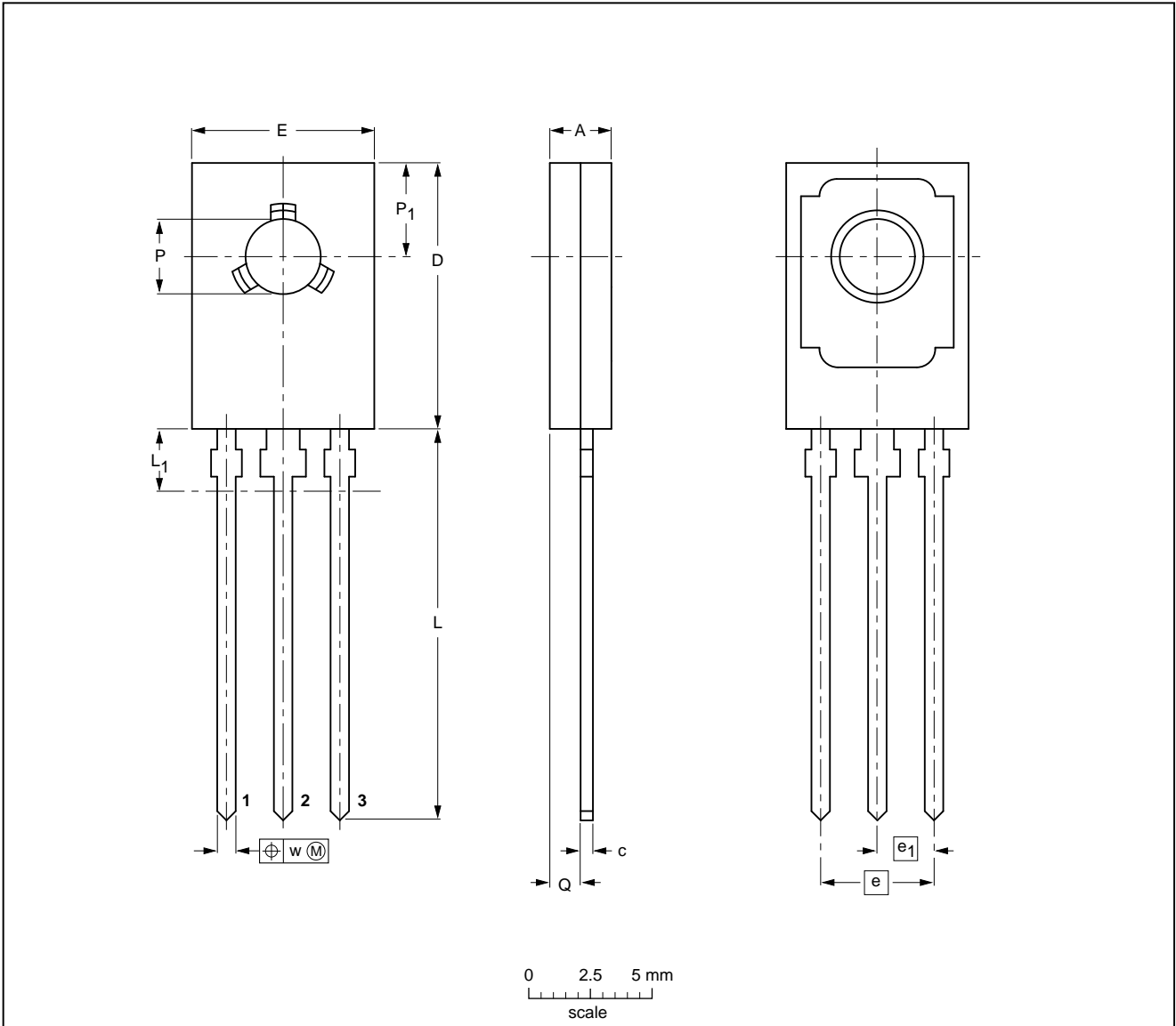


PNP power transistor

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	L	L ₁ ⁽¹⁾ max	Q	P	P ₁	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT32		TO-126				97-03-04

PNP power transistor

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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PNP power transistor

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