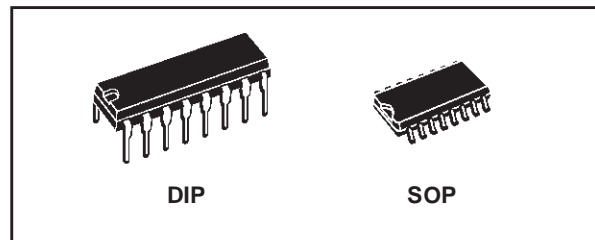


## MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED UP TO 20V
- VERY LOW POWER CONSUMPTION : 70 $\mu$ W (TYP.) AT VCO  $f_o = 10$ kHz,  $V_{DD} = 5$ V
- OPERATING FREQUENCY RANGE : UP TO 1.4MHz (TYP.) AT  $V_{DD} = 10$ V
- LOW FREQUENCY DRIFT : 0.04%/ $^{\circ}$ C (typ.) AT  $V_{DD} = 10$ V
- CHOICE OF TWO PHASE COMPARATORS :
  - 1) EXCLUSIVE - OR NETWORK
  - 2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY: <1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (demod. output)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100$ nA (MAX) AT  $V_{DD} = 18$ V  $T_A = 25^{\circ}$ C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



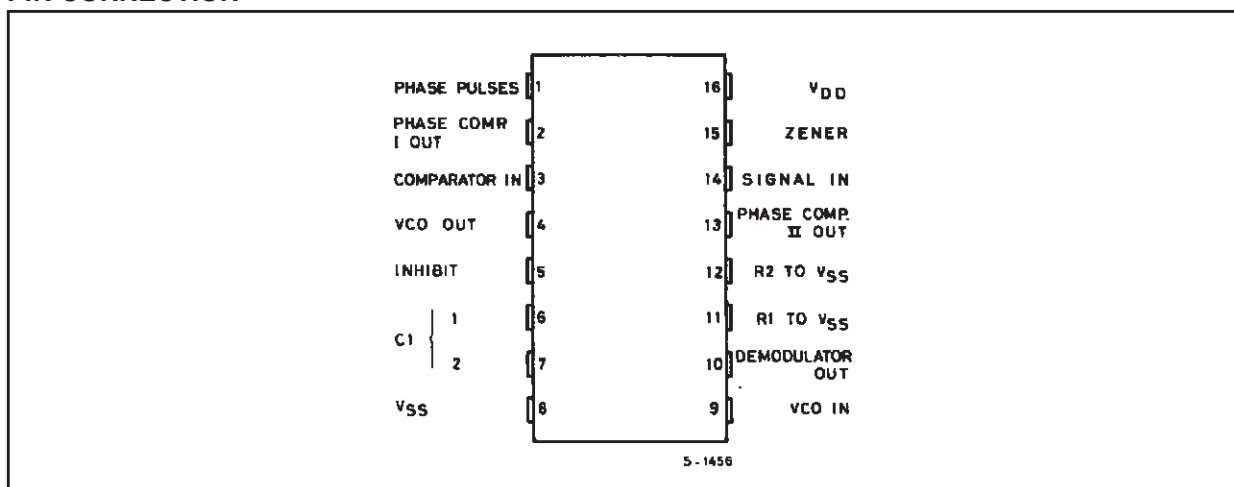
### ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4046BEY	
SOP	HCF4046BM1	HCF4046M013TR

### DESCRIPTION

The HCF4046B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor Technology, available in 16-lead dual in-line plastic or ceramic package. The HCF4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

### PIN CONNECTION



**VCO Section**

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ( $10^{12}\Omega$ ) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMOMULATED OUTPUT). If this terminal is used, a load resistor ( $R_S$ ) of 10 K $\Omega$  or more should be connected from this terminal to  $V_{SS}$ . If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the HCF4024B, HCF4018B, HCF4020B, HCF4022B, HCF4029B and HBF4059A. One or more HCF4018B (Presettable Divide-by-N Counter) or HCF4029B (Presettable Up/Down Counter), or HBF4059A (Programmable Divide-by-"N" Counter), together with the HCF4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

**Phase Comparators**

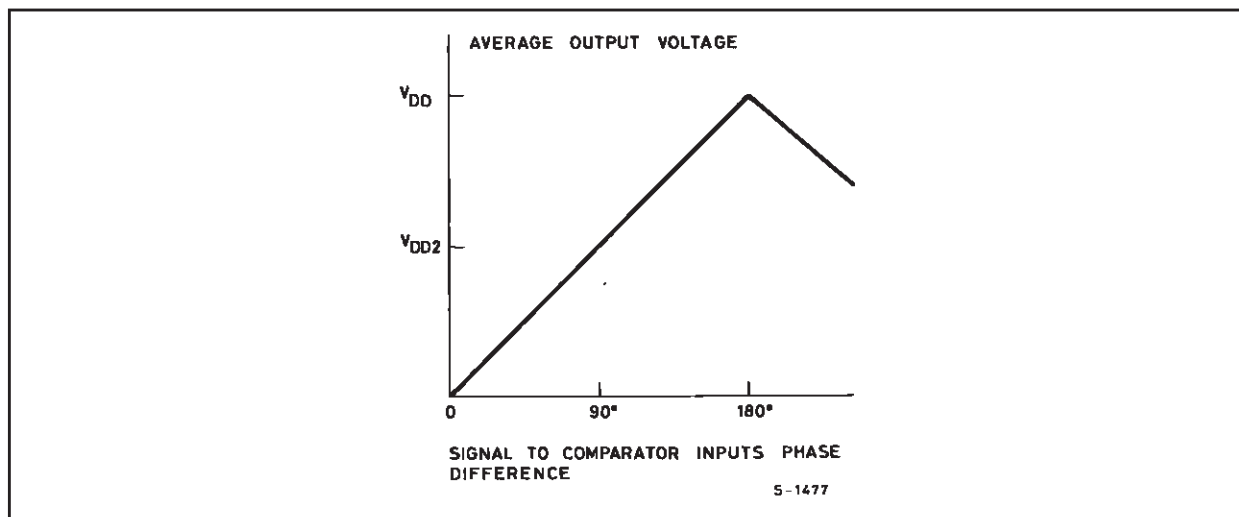
The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0"  $\leq 30\%$  of ( $V_{DD}-V_{SS}$ ), logic "1"  $\geq 70\%$  of ( $V_{DD}-V_{SS}$ )]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to  $V_{DD}/2$ . The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency ( $f_0$ ). The frequency range of

input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ( $2 f_C$ ). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ( $2 f_L$ ). The capture range is  $\leq$  the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between  $0^\circ$  and  $180^\circ$ , and is  $90^\circ$  at the center frequency. Fig.1 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of  $f_0$  is shown in fig.2. Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to  $V_{DD}$  or down to  $V_{SS}$ , respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n- and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the

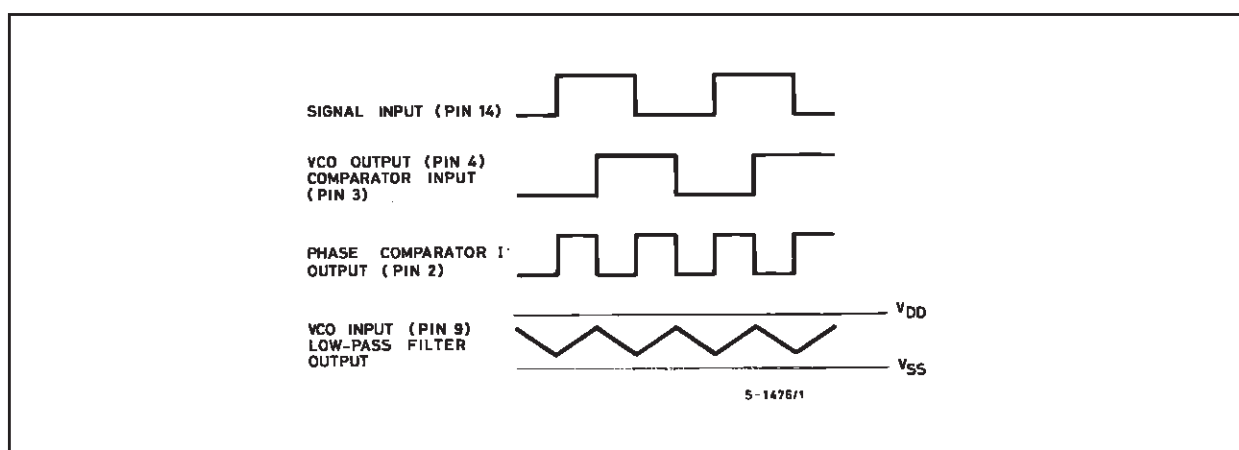
p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between

signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig.3 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

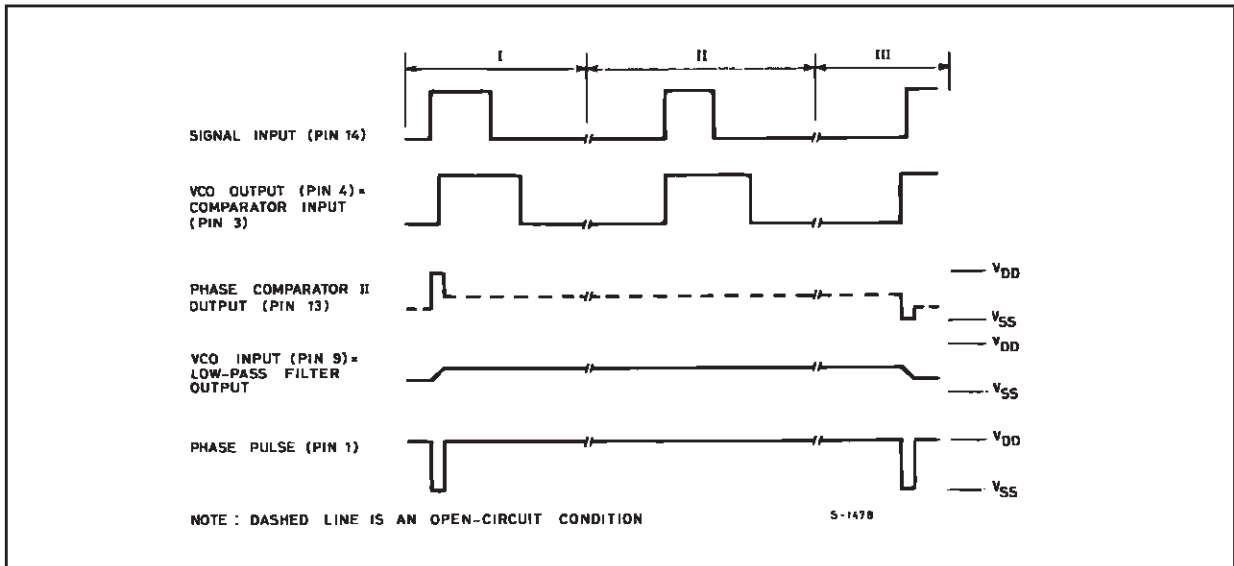
**Figure 1 :** Phase-Comparator I Characteristics at Low-Pass Filter Output.



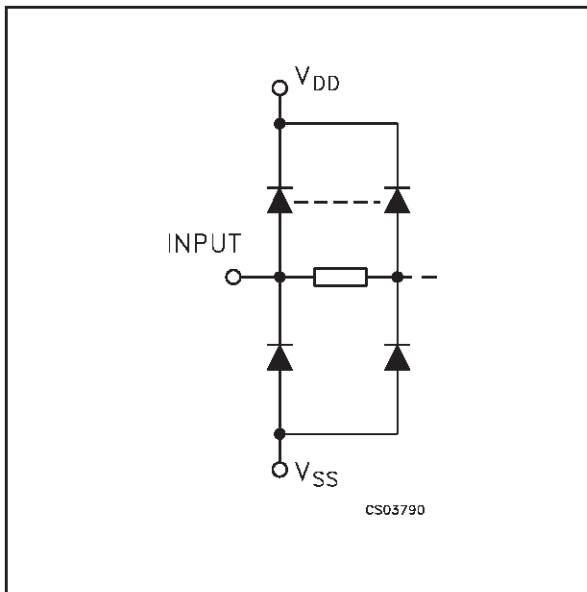
**Figure 2 :** Typical Waveforms for CMOS Phase Locked-Loop Employing Phase Comparator I in Locked Condition of  $f_0$



**Figure 3 :** Typical Waveforms for CMOS Phase-locked Loop Employing Phase Comparator II In Locked Condition



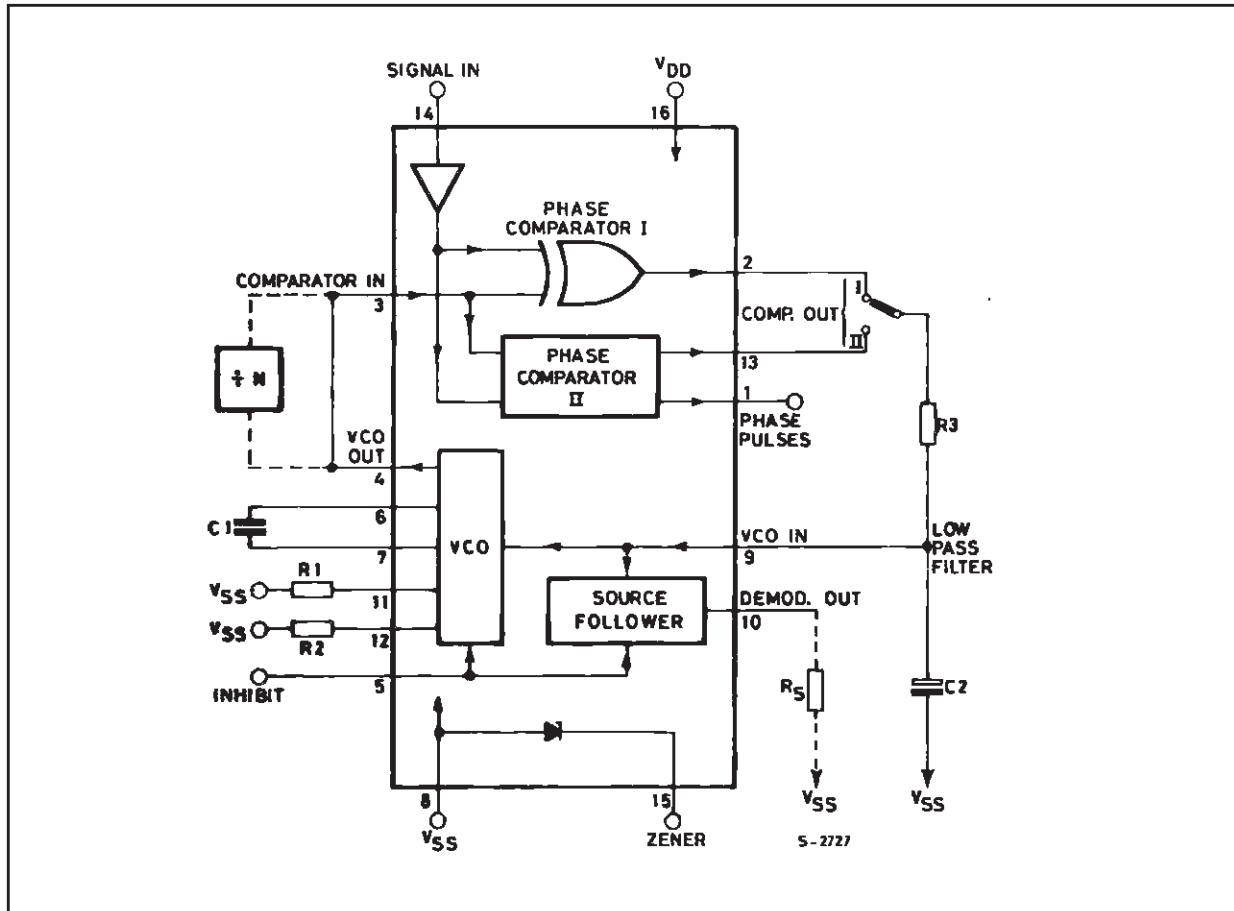
**INPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1	PHASE PULSES	Phase Comparator Pulse Output
2	PHASE COMP I OUT	Phase Comparator 1 Output
3	COMPARATOR IN	Comparator Input
4	VCO OUT	VCO Output
5	INHIBIT	Inhibit Input
6, 7	C1	Capacitors
9	VCO IN	VCO Input
10	DEMODULATOR OUT	Demodulator Output
11	R <sub>1</sub> TO V <sub>SS</sub>	Resistor R1 Connection
12	R <sub>2</sub> TO V <sub>SS</sub>	Resistor R2 Connection
13	PHASE COMP II OUT	Phase Comparator 2 Output
14	SIGNAL IN	Signal Input
15	ZENER	Diode Zener
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to  $V_{SS}$  pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value								Unit
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
<b>VCO SECTION</b>														
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V	
		0/10		<1	10	9.95			9.95		9.95			
		0/15		<1	15	14.95			14.95		14.95			
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V	
		10/0		<1	10		0.05			0.05		0.05		
		15/0		<1	15		0.05			0.05		0.05		
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A	
<b>PHASE COMPARATOR SECTION</b>														
I <sub>DD</sub>	Total Device Current Pin 14= Open Pin 5= V <sub>DD</sub>	0/5			5		0.05	0.1		0.1		0.1	mA	
		0/10			10		0.25	0.5		0.5		0.5		
		0/15			15		0.75	1.5		1.5		1.5		
		0/20			20		2	4		4		4		
	Total Device Current Pin 14= V <sub>SS</sub> or V <sub>DD</sub> Pin 5= V <sub>DD</sub>	0/5			5		0.04	5		150		150	$\mu$ A	
		0/10			10		0.04	10		300		300		
		0/15			15		0.04	20		600		600		
		0/20			20		0.08	100		3000				
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V	
			1/9	<1	10	7			7		7			
			1.5/13.5	<1	15	11			11		11			
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V	
			9/1	<1	10			3		3		3		
			13.5/1.5	<1	15			4		4		4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A	
I <sub>OUT</sub>	High Impedance Leakage Current	0/18	Any Input		18		$\pm 10^{-4}$	$\pm 0.4$		$\pm 12$		$\pm 12$	$\mu$ A	
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF	

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^{\circ}\text{C}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit		
		V <sub>DD</sub> (V)		Min.	Typ.	Max.			
<b>VCO SECTION</b>									
P <sub>D</sub>	Operating Power Dissipation	5	f <sub>O</sub> = 10KHz	R <sub>1</sub> = 10MΩ		70	140	μW	
		10	R <sub>2</sub> = ∞	V <sub>COIN</sub> = V <sub>DD</sub> /2		800	1600		
		15				3000	6000		
f <sub>MAX</sub>	Maximum frequency	5	R <sub>1</sub> = 10KΩ	C <sub>1</sub> = 50pF	0.3	0.6		ns	
		10	R <sub>2</sub> = ∞	V <sub>COIN</sub> = V <sub>DD</sub>	0.6	1.2			
		15			0.8	1.6			
		5	R <sub>1</sub> = 5KΩ	C <sub>1</sub> = 50pF	0.5	0.8		ns	
		10	R <sub>2</sub> = ∞	V <sub>COIN</sub> = V <sub>DD</sub>	1	1.4			
		15			1.4	2.4			
	Center Frequency (f <sub>O</sub> ) and frequency Range f <sub>max</sub> - f <sub>min</sub>	Programable with external components R <sub>1</sub> , R <sub>2</sub> , and C <sub>1</sub> See Design Information							
	Linearity	5	V <sub>COIN</sub> = 2.5V <sup>±0.3</sup>	R <sub>1</sub> = 10KΩ		1.7		%	
		10	V <sub>COIN</sub> = 5V <sup>±1</sup>	R <sub>1</sub> = 100KΩ		0.5			
		10	V <sub>COIN</sub> = 5V <sup>±2.5</sup>	R <sub>1</sub> = 400KΩ		4			
		15	V <sub>COIN</sub> = 7.5V <sup>±1.5</sup>	R <sub>1</sub> = 100KΩ		0.5			
		15	V <sub>COIN</sub> = 7.5V <sup>±5</sup>	R <sub>1</sub> = 1MΩ		7			
	Temperature Frequency Stability (no frequency offset) f <sub>min</sub> = 0	5				±0.12		%/°C	
		10				±0.04			
		15				±0.015			
	Temperature Frequency Stability (frequency offset) f <sub>min</sub> = 0	5					±0.09		
		10					±0.07		
		15					±0.03		
VCO	Output Duty Cycle	5, 10, 15				50		%	
t <sub>TLH</sub> t <sub>THL</sub>	VCO Output Transition Time	5				100	200	ns	
		10				50	100		
		15				40	80		
	Source Follower Output (Demodulated Output): Offset Voltage V <sub>COIN</sub> -V <sub>DEM</sub>	5, 10, 15	R <sub>S</sub> > 10KΩ			1.8	2.5	V	
	Source Follower Output (Demodulated Output): Linearity	5	R <sub>S</sub> = 100KΩ	V <sub>COIN</sub> = 2.5V <sup>±0.3</sup>		0.3		%	
		10	R <sub>S</sub> = 300KΩ	V <sub>COIN</sub> = 5V <sup>±2.5</sup>		0.7			
		15	R <sub>S</sub> = 500KΩ	V <sub>COIN</sub> = 7.5V <sup>±5</sup>		0.9			
V <sub>Z</sub>	Zener Diode Voltage		I <sub>Z</sub> = 50 μA		4.45	5.5	7.5	V	
R <sub>Z</sub>	Zener Dynamic Resistance		I <sub>Z</sub> = 1 mA			40		Ω	

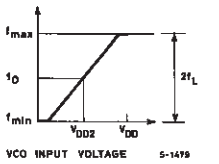
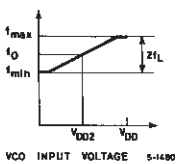
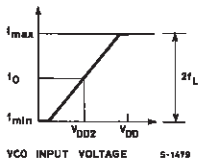
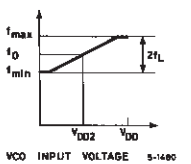
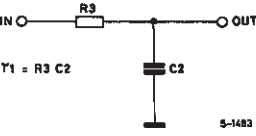
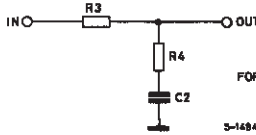
## HCF4046B

Symbol	Parameter	Test Condition		Value (*)			Unit
		V <sub>DD</sub> (V)		Min.	Typ.	Max.	
<b>PHASE COMPARATOR SECTION</b>							
R14	Pin 14 (signal in) Input Resistance	5		1	2		MΩ
		10		0.2	0.4		
		15		0.1	0.2		
	AC Coupled Signal Input Sensivity (*) (peak to peak)	5	f <sub>IN</sub> = 100KHz sine wave		180	360	mV
		10			330	660	
		15			900	1800	
t <sub>PLH</sub>	Propagation Delay Time High to Low Level Pins 14 to 1	5			225	450	ns
		10			100	200	
		15			65	130	
t <sub>PLH</sub>	Propagation Delay Time Low to High Level	5			350	700	ns
		10			150	300	
		15			100	200	
t <sub>PHZ</sub>	Disable Time High Level to High Impedance Pins 14 to 13	5			225	450	ns
		10			100	200	
		15			65	130	
t <sub>PLZ</sub>	Disable Time Low Level to High Impedance	5			285	570	ns
		10			130	260	
		15			95	190	
t <sub>r</sub> t <sub>f</sub>	Input Rise or Fall Time Comparator Pin 3	5				50	μs
		10				1	
		15				0.3	
	Signal Pin 14	5				500	μs
		10				20	
		15				2.5	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	

(\*) For sine Wave the frequency must be greater than 10KHz for Phase Comparator II



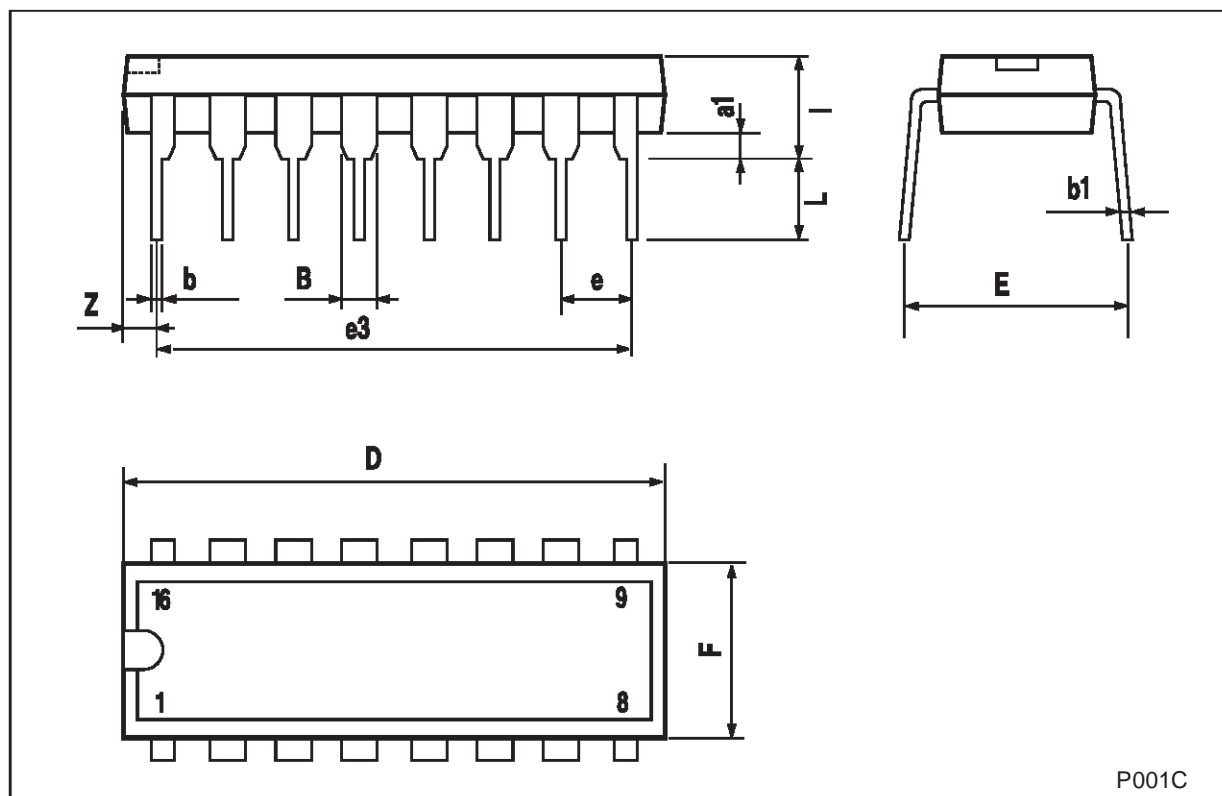
**DESIGN INFORMATION** This information is a guide for approximating the value of external components in a Phase-Locked-Loop system. The selected external components must be within the following ranges:  $5K\Omega \leq R_1, R_2, R_S \leq 1M\Omega$   $C_1 \geq 100pF$  at  $V_{DD} \geq 5V$   $C_1 \geq 50pF$  at  $V_{DD} \geq 10V$

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2=\infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2=\infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL System will Adjust to Centre Frequency $f_0$		VCO in PLL System will Adjust to Lowest Operating Frequency $f_0$	
Frequency Lock Range, $2f_L$	$2f_L = \text{Full VCO Frequency Range}$ $2f_L = f_{max} - f_{min}$			
Frequency Lock Range, $2f_C$	 <p><math>\tau_1 = R_3 C_2</math></p> <p>(1), (2)</p> <p><math>2f_C \approx \frac{1}{\pi \tau_1} \sqrt{\frac{2\tau_1 f_L}{\tau_1}}</math></p>		$f_C = f_L$	
Loop filter Component Section	 <p>FOR <math>2f_C</math> SEE REF. (2)</p>			
Phase Angle Between Signal and Comparator	90° at Centre frequency ( $f_0$ ), approximating 0° and 180° at ends of lock range ( $2f_L$ )		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

For further information, see  
 (1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966  
 (2) G.S. Moskytz "miniaturized RC filters using phase Lockedloop" BSTJ May 1965

## Plastic DIP-16 (0.25) MECHANICAL DATA

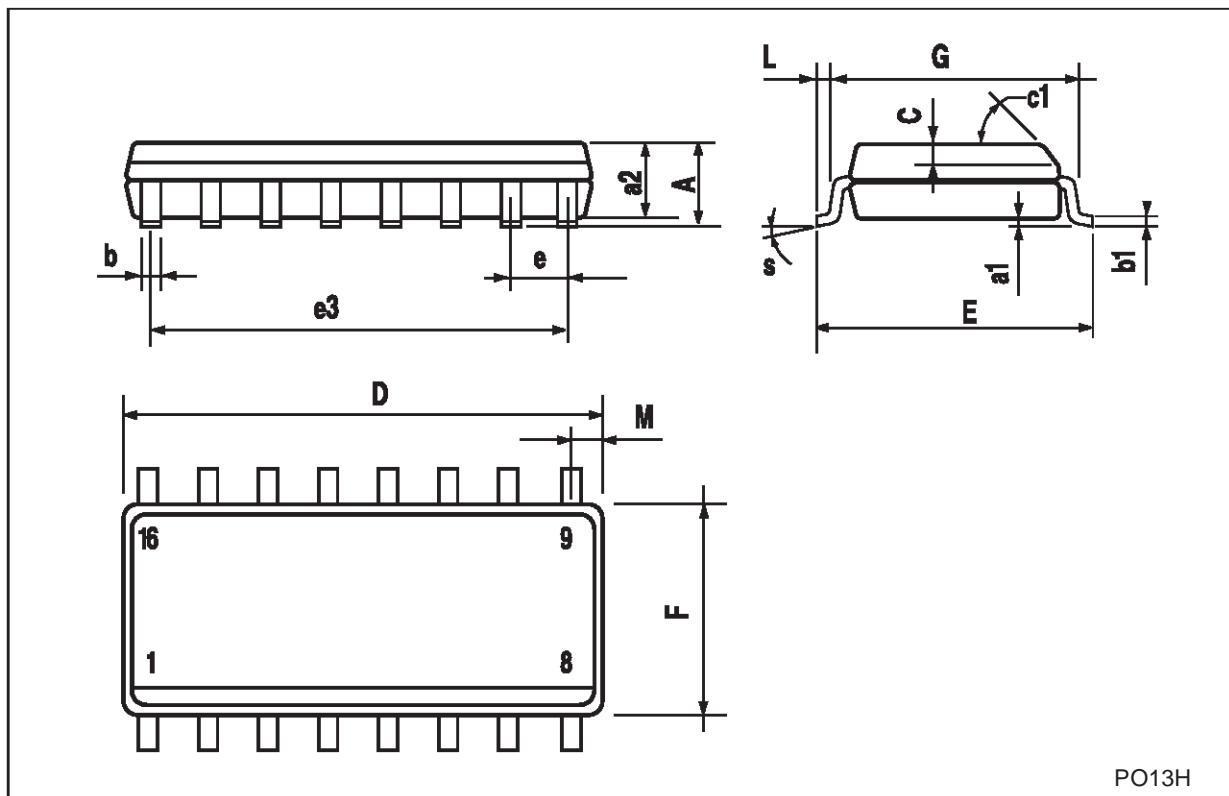
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

## SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

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