

PowerMOS transistor

BUK445-600B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic full-pack envelope. The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

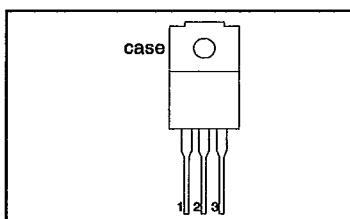
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	2.2	A
P_{tot}	Total power dissipation	30	W
$R_{DS(ON)}$	Drain-source on-state resistance	2.5	Ω

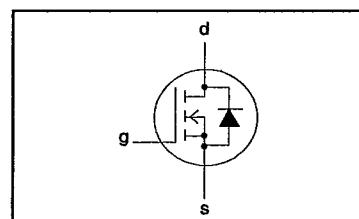
PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	600	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	600	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	$T_{hs} = 25^\circ\text{C}$	-	2.2	A
I_D	Drain current (DC)	$T_{hs} = 100^\circ\text{C}$	-	1.4	A
I_{DM}	Drain current (pulse peak value)	$T_{hs} = 25^\circ\text{C}$	-	8.8	A
P_{tot}	Total power dissipation	$T_{hs} = 25^\circ\text{C}$	-	30	W
T_{stg}	Storage temperature	$T_{hs} = 25^\circ\text{C}$	-55	150	$^\circ\text{C}$
T_J	Junction Temperature	-	-	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-hs)}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.1	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient		-	55	-	K/W

Philips Semiconductors

Product Specification

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STATIC CHARACTERISTICS $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 0.25 \text{ mA}$	600	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25^\circ\text{C}$	-	2	20	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125^\circ\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 30 \text{ V}; V_{DS} = 0 \text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 2.5 \text{ A}$	-	2.1	2.5	Ω

DYNAMIC CHARACTERISTICS $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_f	Forward transconductance	$V_{DS} = 25 \text{ V}; I_D = 2.5 \text{ A}$	2.5	4.5	-	S
C_{iss}	Input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz}$	-	750	1000	pF
C_{oss}	Output capacitance		-	90	140	pF
C_{rss}	Feedback capacitance		-	40	70	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30 \text{ V}; I_D = 2.6 \text{ A}; V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega; R_{gen} = 50 \Omega$	-	10	45	ns
t_r	Turn-on rise time		-	45	60	ns
$t_{d(off)}$	Turn-off delay time		-	100	140	ns
t_f	Turn-off fall time		-	40	65	ns
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. $\leq 65\%$; clean and dustfree	-	-	1500	V
C_{isol}	Capacitance from T2 to external heatsink	$f = 1 \text{ MHz}$	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_{hs} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	2.5	A
I_{DPM}	Pulsed reverse drain current	-	-	-	10	A
V_{SD}	Diode forward voltage	$I_F = 2.5 \text{ A}; V_{GS} = 0 \text{ V}$	-	1.1	1.4	V
t_r	Reverse recovery time	$I_F = 2.5 \text{ A}; -dI_F/dt = 100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_R = 100 \text{ V}$	-	1200	-	ns
Q_r	Reverse recovery charge		-	6.0	-	μC

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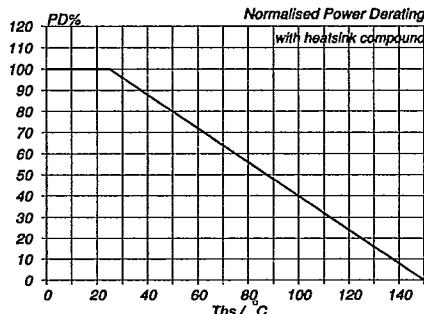


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_{hs})$

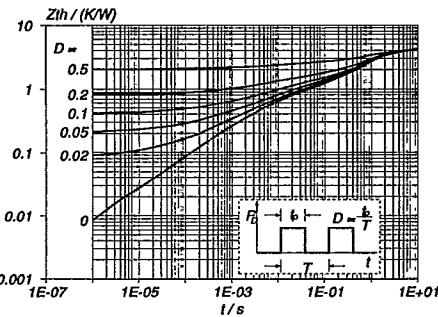


Fig.4. Transient thermal impedance.
 $Z_{th\ j-hs} = f(t); \text{parameter } D = t_p/T$

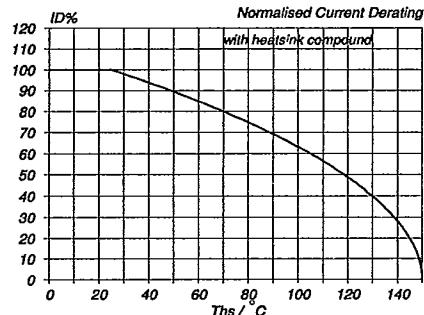


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_{hs}); \text{conditions: } V_{GS} \geq 10 \text{ V}$

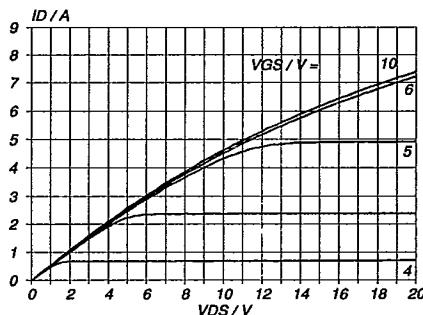


Fig.5. Typical output characteristics, $T_J = 25^\circ C$.
 $I_D = f(V_{DS}); \text{parameter } V_{GS}$

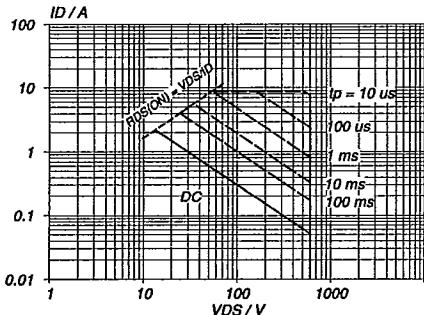


Fig.3. Safe operating area. $T_{hs} = 25^\circ C$
 $I_D \& I_{DM} = f(V_{DS}); I_{DM} \text{ single pulse}; \text{parameter } t_p$

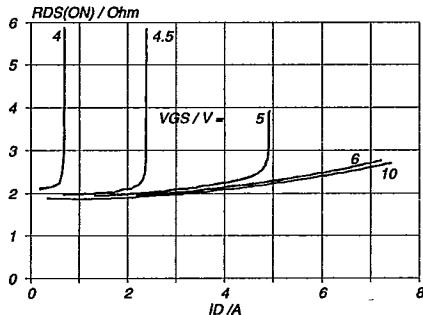


Fig.6. Typical on-state resistance, $T_J = 25^\circ C$.
 $R_{DS(ON)} = f(I_D); \text{parameter } V_{GS}$

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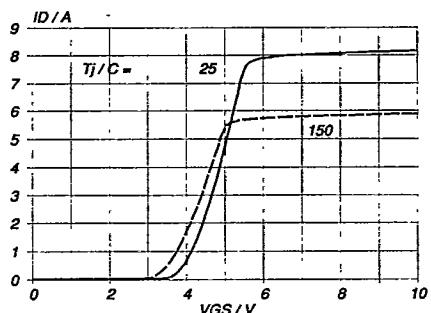


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25 \text{ V}$; parameter T_J

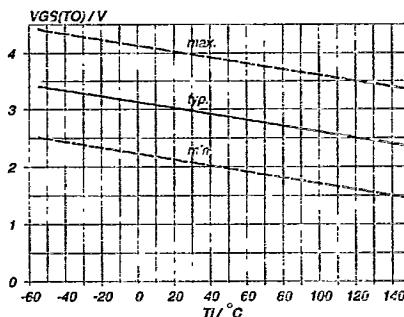


Fig.10. Gate threshold voltage.
 $V_{GS(To)} = f(T_J)$; conditions: $I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

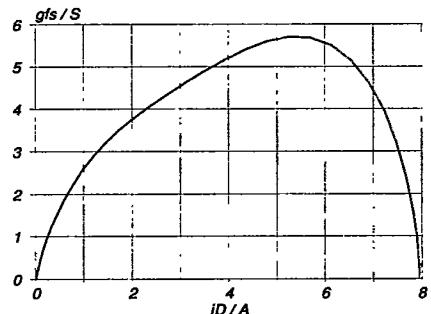


Fig.8. Typical transconductance, $T_J = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25 \text{ V}$

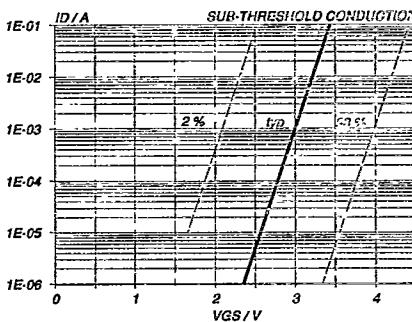


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_J = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

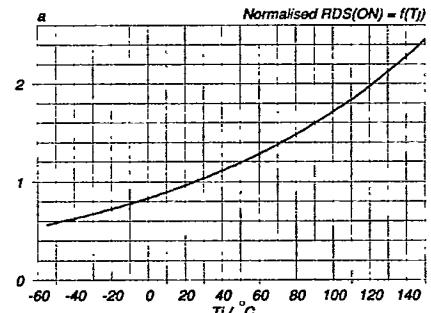


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(on)} / R_{DS(ON)25^\circ\text{C}} = f(T_J)$; $I_D = 2.5 \text{ A}$; $V_{GS} = 10 \text{ V}$

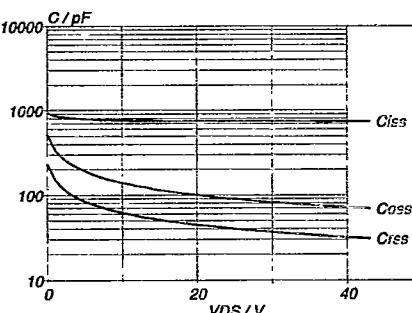


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

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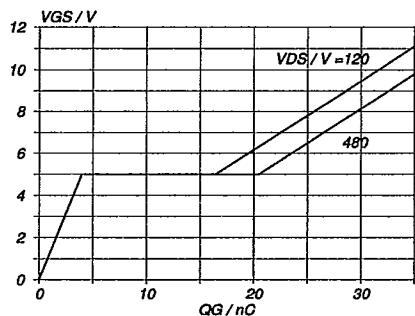


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 4.5 \text{ A}$; parameter V_{DS}

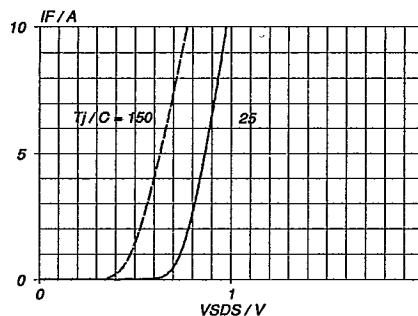


Fig.14. Typical reverse diode current.
 $I_F = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; parameter T_J