TEMIC

Siliconix

DG201A/202

Monolithic Quad SPST Analog Switches

Features

- ±15-V Input Range
- Low Off Leakage—$I_{D(on)}$: 0.1 nA
- Low On-Resistance—$r_{DS(on)}$: 115 Ω
- 44-V Maximum Supply Ratings
- TTL and CMOS Compatible

Benefits

- Wide Input Range
- Low Distortion Switching
- Can Be Driven from Comparators or Op Amps Without Limiting Resistors

Applications

- Disk Drives
- Radar Systems
- Communications Systems
- Sample-and-Hold

Description

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. When combining a low on-resistance and a wide signal range (±15 V) with low charge-transfer these devices are well suited for industrial and military applications.

Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch conducts equally well in both directions when on. When off these switches will block up to 30 V peak-to-peak and have a 44-V absolute maximum power supply rating.

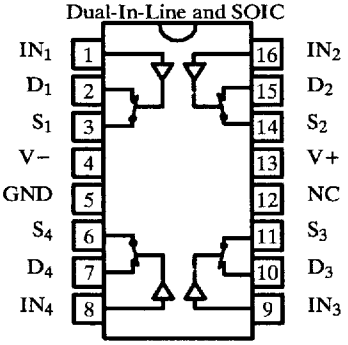
These two devices are differentiated by the type of switch actions (See Truth Table).

The DG201B/DG202B upgrades are recommended for new designs.

Functional Block Diagram and Pin Configuration

DG201A

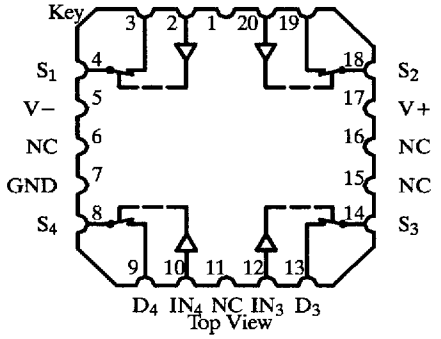
Dual-In-Line and SOIC



Top View

DG201A

LCC



Top View

Ordering Information – DG201A/202

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG201ACJ/DG202CJ
−25 to 85°C	16-Pin CerDIP	DG201ABK
−40 to 85°C	16-Pin Narrow SOIC	DG201ADY
−55 to 125°C	16-Pin CerDIP	DG201AAK
		DG201AAK/883, JM38510/12302BEA
		7705301EA
		DG202AK/DG202AK/883
	16-Pin Sidebraze	JM38510/12302BEC
		7705301EC
	LCC-20	77053012A

Truth Table

Logic	DG201A	DG202
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 VSwitches Shown for DG201A Logic "0" Input

Absolute Maximum Ratings

Voltages Referenced to V−

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[a] V_S, V_D ..... (V−) −2 V to (V+) +2 V
or 20 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (K, Z Suffix) ..... −65 to 150°C
(J, Y Suffix) ..... −65 to 125°C

Power Dissipation (Package)b

16-Pin Plastic DIP[c] ..... 470 mW
16-Pin SOIC[d] ..... 640 mW
16-Pin CerDIP and Sidebraze[e] ..... 900 mW
LCC-20[f] ..... 750 mW

Notes
a. Signals on S_X, D_X, or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C
f. Derate 10 mW/°C above 75°C

Specifications[a]

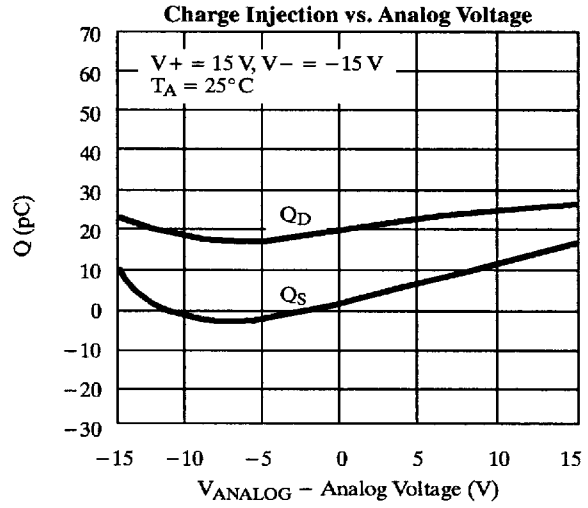
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix Min[d]	B, C, D Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = 1 mA	Room	115		175		175	Ω
			Full			250		250	
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room	±0.02	−1	1	−5	5	nA
			Full		−100	100	−100	100	
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±14 V, V_S = ∓14 V	Room	±0.02	−1	1	−5	5	
			Full		−100	100	−100	100	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room	±0.15	−1	1	−5	5	
			Full		−200	200	−200	200	
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4 V	Room	−0.0004	−1		−1		µA
			Full		−1		−10		
		V_{IN} = 15 V	Room	0.003		1		1	
			Full			10		10	
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room	−0.0004	−1		−1		
			Full		−10		−10		
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Switching Time Test Circuit	Room	480		600		600	ns
Turn-Off Time	t_{OFF}		Room	370		450		450	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V R_g = 0 Ω	Room	20					pC
Source-Off Capacitance	$C_{S(off)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)}$ + $C_{S(on)}$	V_D = V_S = 0 V, V_{IN} = 0 V f = 1 MHz	Room	16					
Off Isolation	OIRR	V_{IN} = 5 V, R_L = 75 Ω V_S = 2 V, f = 100 kHz	Room	70					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	90					

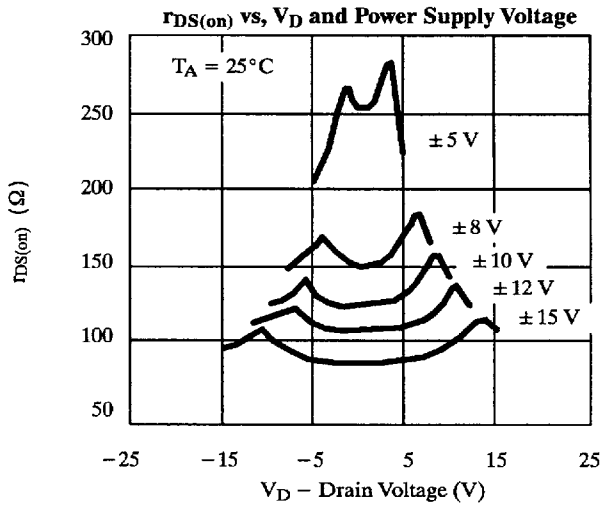
Specifications[a] (Cont'd)

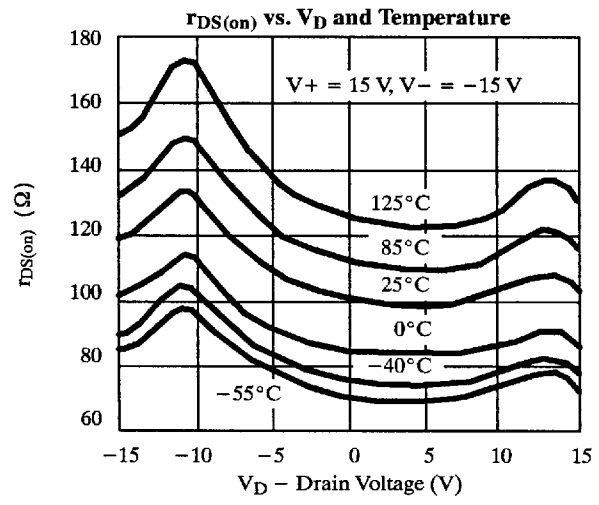
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15V V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	B, C, D Suffix Min[d]	B, C, D Suffix Max[d]	Unit
Power Supply									
Positive Supply Current	I+	All Channels On or Off	Room	0.9		2		2	mA
Negative Supply Current	I−		Room	−0.3	−1		−1		

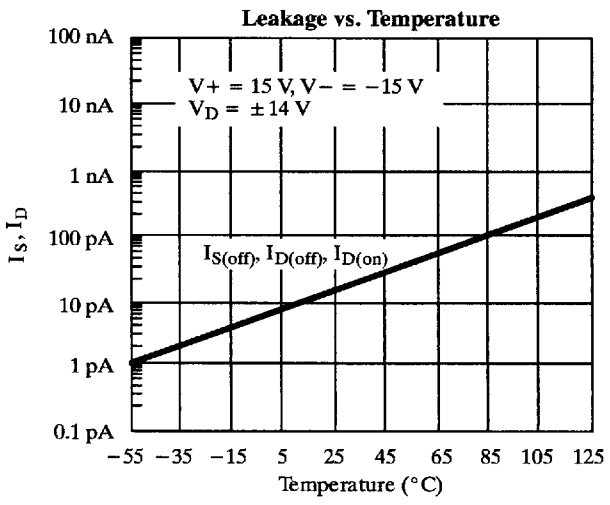
Notes
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics



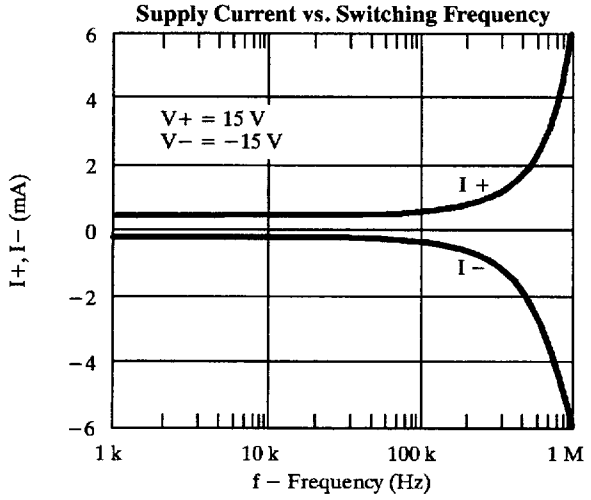




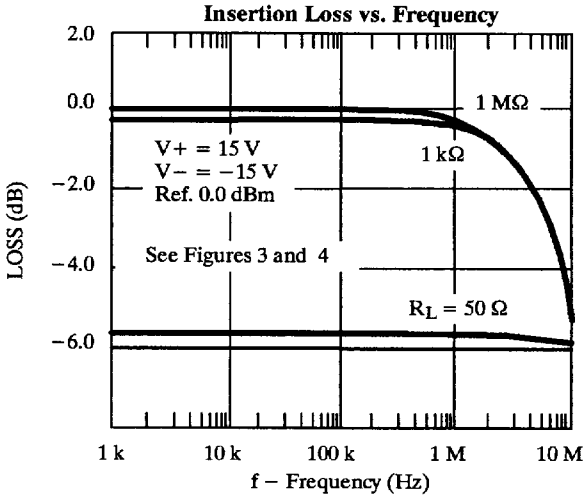


Typical Characteristics (Cont'd)

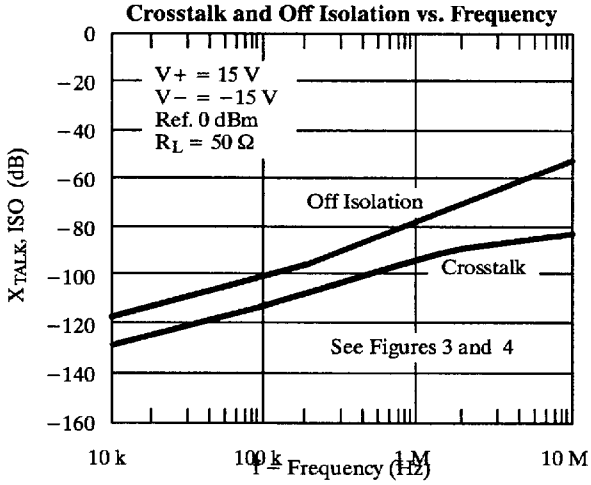
Supply Current vs. Switching Frequency



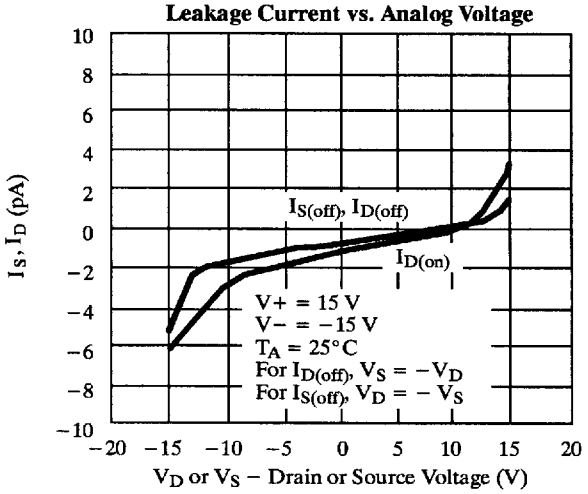
Insertion Loss vs. Frequency



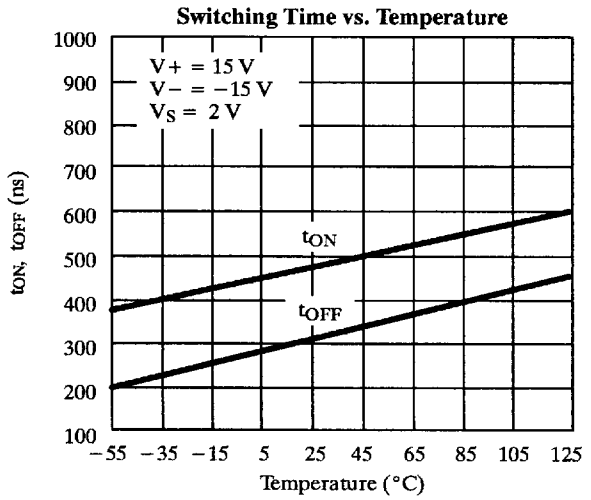
Crosstalk and Off Isolation vs. Frequency



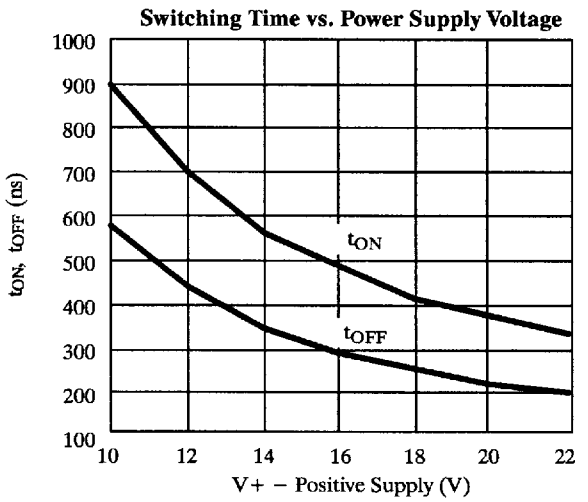
Leakage Current vs. Analog Voltage



Switching Time vs. Temperature



Switching Time vs. Power Supply Voltage



Schematic Diagram (Typical Channel)

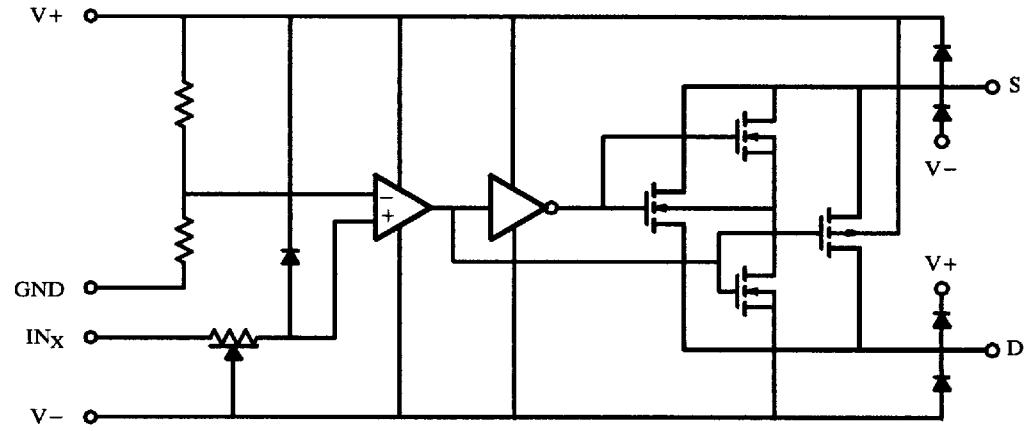


Figure 1.

Test Circuits

V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

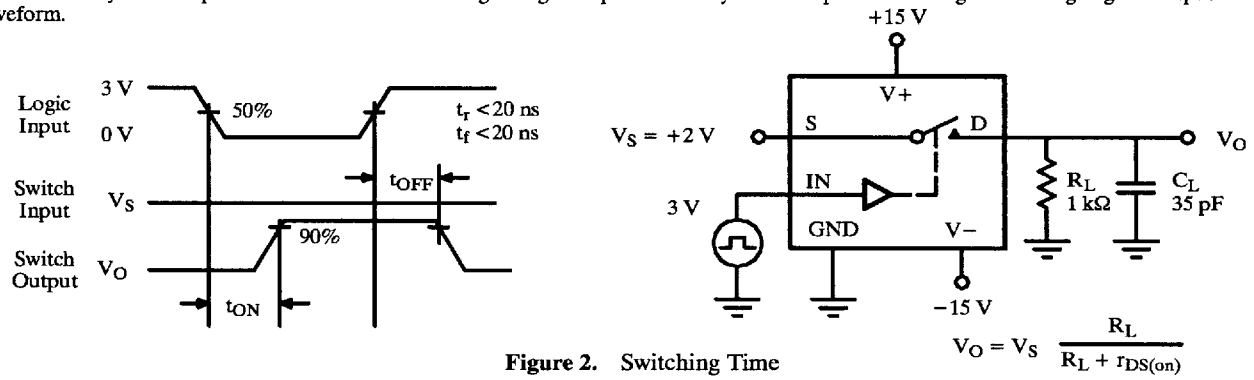


Figure 2. Switching Time

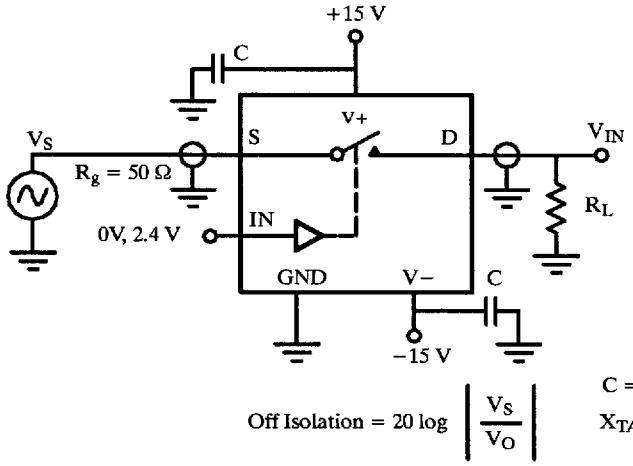


Figure 3. Off Isolation

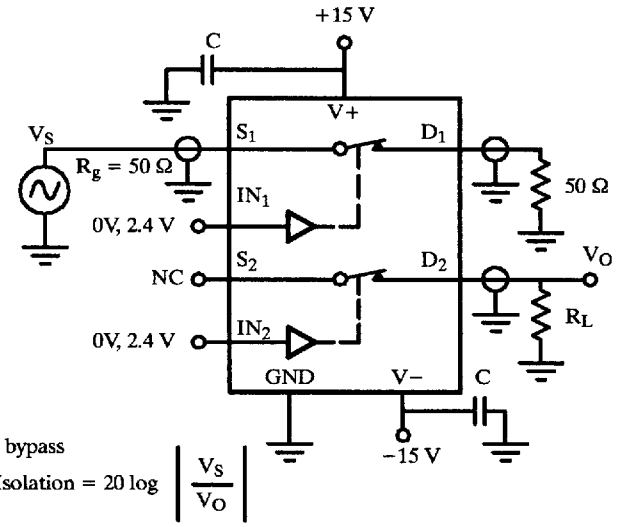
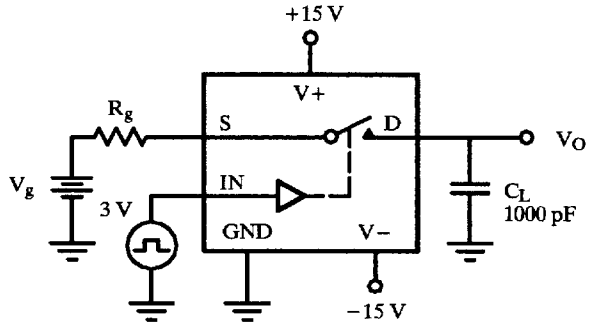
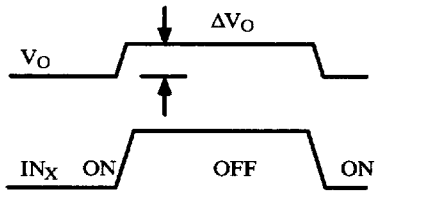


Figure 4. Channel-to-Channel Crosstalk

Test Circuits (Cont'd)





ΔV_O = measured voltage error due to charge injectic
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$

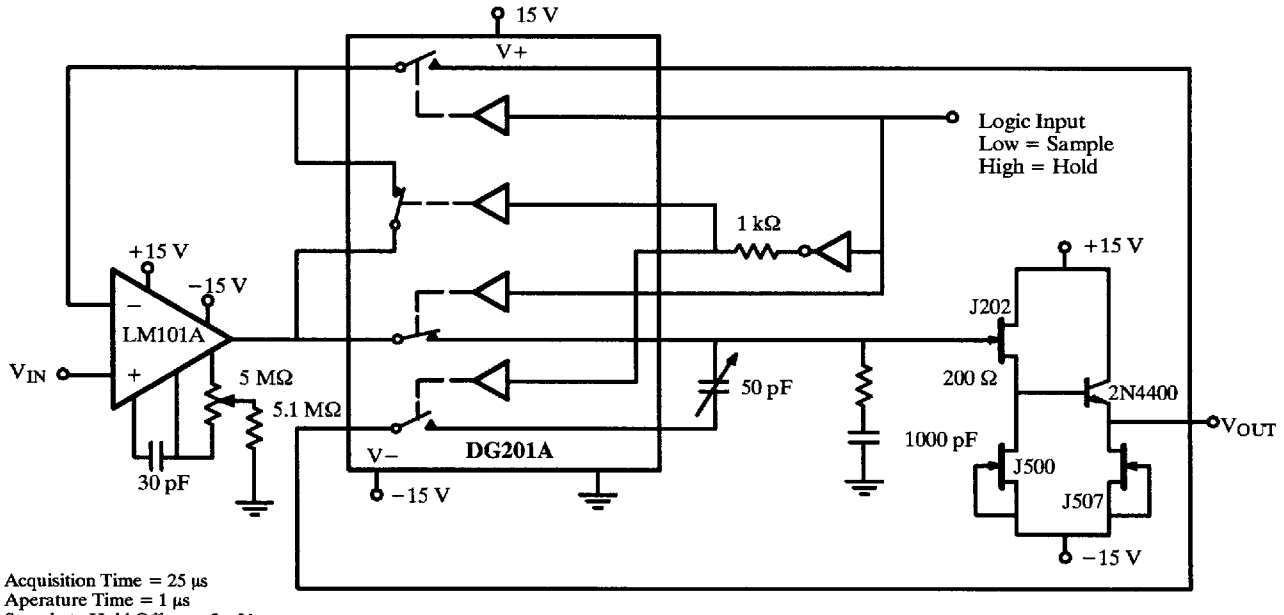
Figure 5. Charge Injection

Application Hints[a]

V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	−15	2.4/0.8	−15 to 15
10	−12	2.4/0.8	−12 to 12
12	−10	2.2/0.6	−10 to 10
8[b]	−8	2.0/0.5	−8 to 8

Notes
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
b. Operation below ±8 V is not recommended.

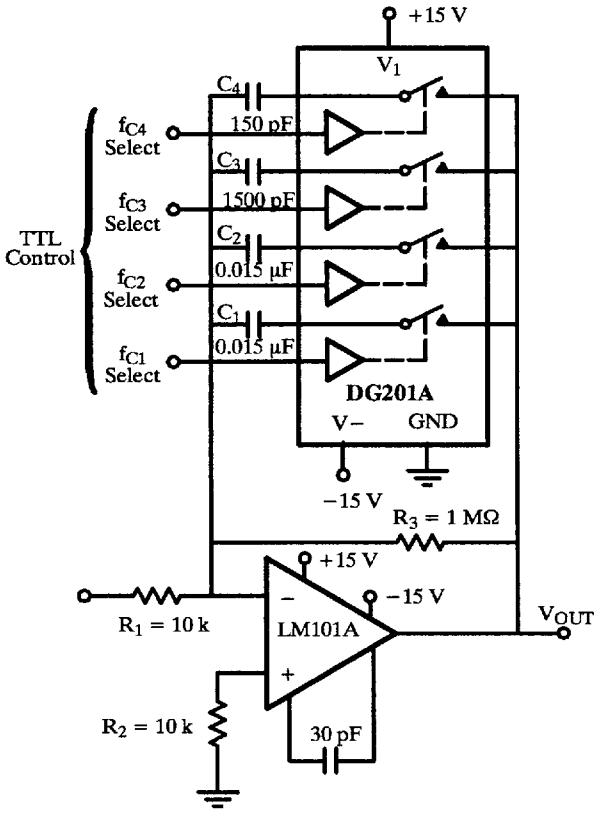
Applications

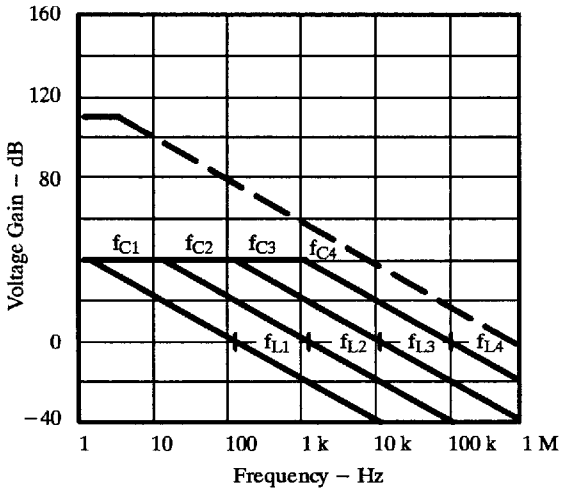


Acquisition Time = 25 µs
Aperature Time = 1 µs
Sample to Hold Offset = 5 mV
Droop Rate = 5 mV/s

Figure 6. Sample-and-Hold

Applications (Cont'd)





A_L (Voltage Gain Below Break Frequency) = $\frac{R_3}{R_1}$ = 100 (40 dB)

f_C (Break Frequency) = $\frac{1}{2\pi R_3 C_X}$

f_L (Unity Gain Frequency) = $\frac{1}{2\pi R_1 C_X}$

Max Attenuation = $\frac{r_{DS(on)}}{10\text{ k}} \approx -40$ dB

Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

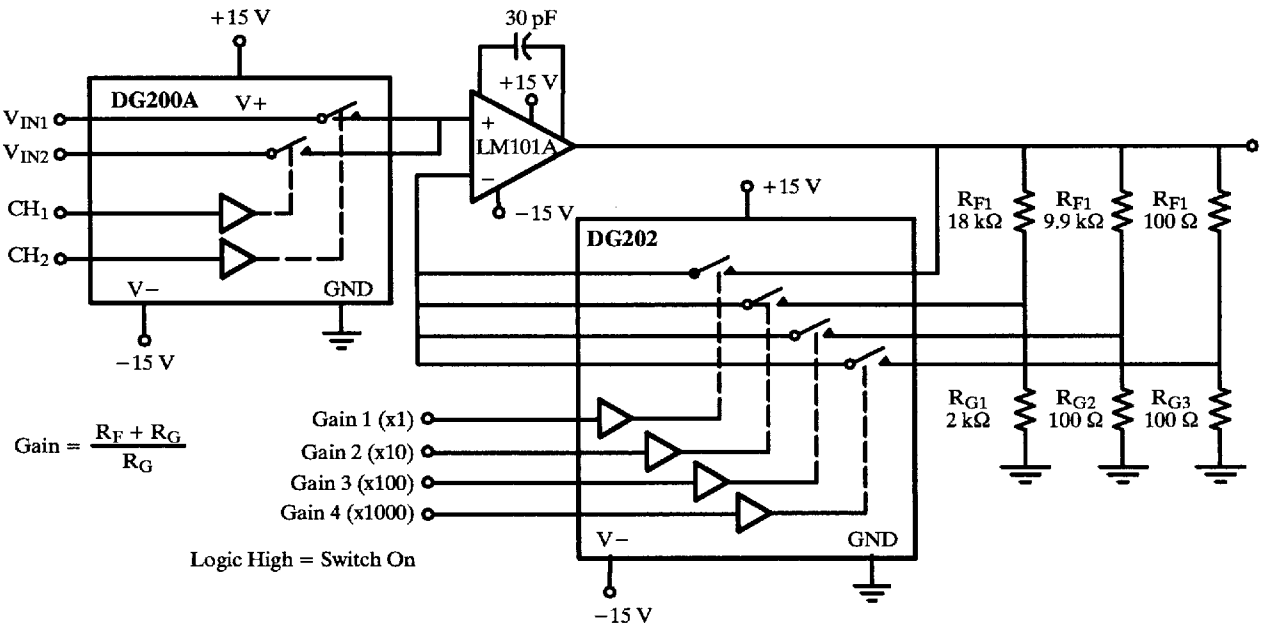


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains