



**GoldStar**  
GOLDSTAR ELECTRON CO., LTD.

# GM76C256AL/ALL

32,768 WORDS × 8 BIT  
CMOS STATIC RAM

## Description

The GM76C256AL/ALL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 50mA (max) at minimum cycle time of 70ns.

When  $\overline{CS}$  is a logical high, the device is placed in low power standby mode in which standby current is 1mA (max).

The GM76C256AL/ALL has two control inputs. Chip select ( $\overline{CS}$ ) allows for device selection and data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access.

Thus the GM76C256AL/ALL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256AL/ALL is offered in 28 pin DIP (600 mil), SOP (330 mil) and TSOP 1 (0814).

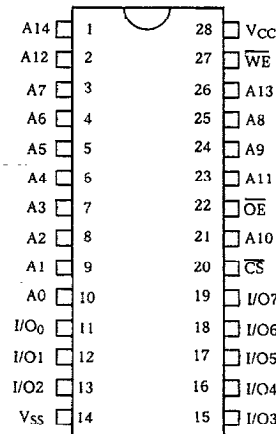
## Features

- High Speed; Fast Access and Cycle Time 70/85/100ns Max.
- Low Power Standby and Low Power Operation; Stand by: 0.55mW Max. (Low Power Version) Stand by: 0.17mW Max. (Low Low Power Version) Operation: 275mW Max.
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Standard 28 DIP, SOP and TSOP I

## Pin Description

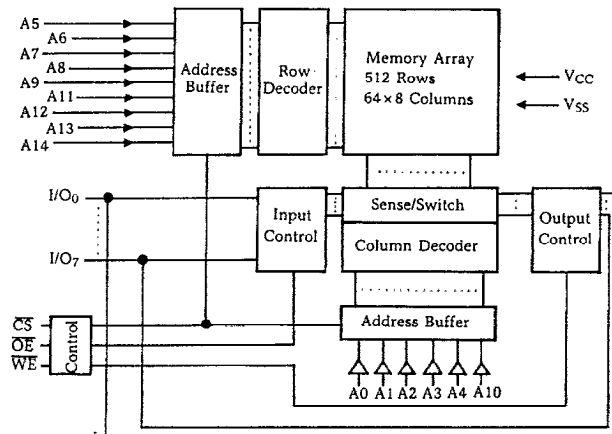
Pin	Function
A0 ~ A14	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$	Chip Select Input
I/O0 ~ I/O7	Data Input/Output
V <sub>CC</sub>	Power Supply +5V
V <sub>SS</sub>	Ground

## Pin Configuration



(Top View)

## Block Diagram



**Absolute Maximum Ratings\***

Symbol	Parameter	Rating	Unit
T <sub>A</sub>	Ambient Temperature under Bias	0 ~ 70	°C
T <sub>STC</sub>	Storage Temperature	-65 ~ 150	°C
T <sub>SOL</sub>	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V <sub>CC</sub>	Supply Voltage	-0.3 ~ 7.0	V
V <sub>IN</sub>	Input Voltage	-0.3* ~ 7.0	V
V <sub>I/O</sub>	Input and Output Voltage	-0.5 ~ V <sub>CC</sub> +0.5	V
P <sub>D</sub>	Power Dissipation	1.0	W

\*: -3.0V at pulse width 50ns Max.

**Recommended Operating Conditions (T<sub>A</sub>=0 ~ 70°C)**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.2	—	V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	—	0.8	V
V <sub>DR</sub>	Data Retention Supply Voltage	2.0	—	5.5	V

**Truth Table**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Note: X means don't care

**DC Electrical Characteristics: (V<sub>CC</sub>=5V ± 10%, T<sub>A</sub>=0 ~ 70°C)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1.0mA	2.4	—	—	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	—	—	0.4	V
I <sub>I(L)</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	—	1	μA
I <sub>O(L)</sub>	Output Leakage Current	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ , V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	-1	—	1	μA
I <sub>CCS1</sub>	Stand-by Power Supply Current	$\overline{CS} = V_{IH}$	—	—	1	mA
I <sub>CCS2</sub>		$\overline{CS} \geq V_{CC} - 0.2V$ GM76C256AL GM76C256ALL	—	2* 1*	100 20	μA μA
I <sub>CC</sub>	Operating Supply Current	$\overline{CS} = V_{IL}$ , V <sub>I/O</sub> = 0mA	—	7	15	mA
I <sub>CC1</sub>	Average Operating Power Supply Current	Min. Cycle, duty = 100% I <sub>I/O</sub> = 0mA	—	—	50	mA

\*TYP. Values are measured at 25°C, V<sub>CC</sub>=5V

AC Operating Characteristics ( $V_{CC}=5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ\text{C}$ )

## Read Cycle

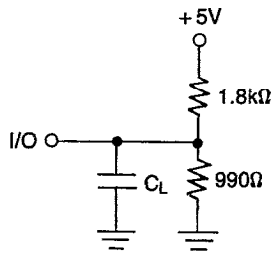
Symbol	Parameter	Conditions	GM76C256AL-70		GM76C256AL-85		GM76C256AL-10		Unit
			Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	*1	70	—	85	—	100	—	ns
$t_{AA}$	Address Access Time		—	70	—	85	—	100	ns
$t_{ACS}$	Chip Select Access Time		—	70	—	85	—	100	ns
$t_{OE}$	Output Enable to Output Valid		—	35	—	45	—	50	ns
$t_{OH}$	Output Hold from Address Change		5	—	5	—	10	—	ns
$t_{CLZ}$	Chip Selection to Output in Low-Z	*2	10	—	10	—	10	—	ns
$t_{OLZ}$	Output Enable to Output in Low-Z		5	—	5	—	5	—	ns
$t_{CHZ}$	Chip Deselection to Output in High-Z		0	30	0	30	0	35	ns
$t_{OHZ}$	Output Disable to Output in High-Z		0	30	0	30	0	35	ns

## Write Cycle

Symbol	Parameter	Conditions	GM76C256AL-70		GM76C256AL-85		GM76C256AL-10		Unit
			Min	Max	Min	Max	Min	Max	
$t_{WC}$	Write Cycle Time	*1	70	—	85	—	100	—	ns
$t_{CW}$	Chip Selection to End of Write		60	—	75	—	80	—	ns
$t_{AW}$	Address Valid to End of Write		60	—	75	—	80	—	ns
$t_{AS}$	Address Setup Time		0	—	0	—	0	—	ns
$t_{WP}$	Write Pulse Width		50	—	60	—	60	—	ns
$t_{WR}$	Write Recovery Time		0	—	5	—	5	—	ns
$t_{DW}$	Data to Write Time Overlap		30	—	40	—	40	—	ns
$t_{DH}$	Data Hold from Write Time		0	—	0	—	0	—	ns
$t_{WHZ}$	Write to Output in High-Z	*2	0	25	0	30	0	35	ns
$t_{OW}$	Output Active from End of Write		5	—	5	—	5	—	ns

**\*1 Test Conditions**

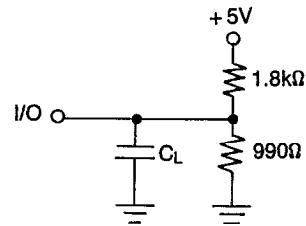
1. Input pulse level: 0.6V to 2.4V
2.  $t_r = t_f = 5\text{ns}$
3. Input and output timing reference levels: 1.5V
4. Output load  $C_L = 100\text{pF}$



$C_L = 100\text{pF}$  (Includes Jig Capacitance)

**\*2 Test Conditions**

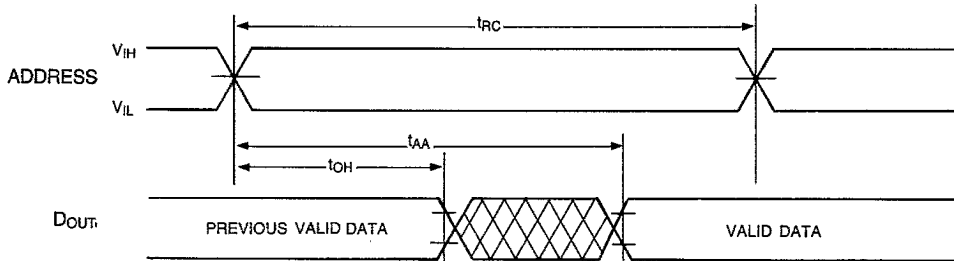
1. Input pulse level: 0.6V to 2.4V
2.  $t_r = t_f = 5\text{ns}$
3. Input timing reference level: 0.8V to 2.2V.
4. Output timing reference levels:  
 $\pm 200\text{mV}$  (the level displace from stable output voltage level)
5. Output load  $C_L = 5\text{pF}$



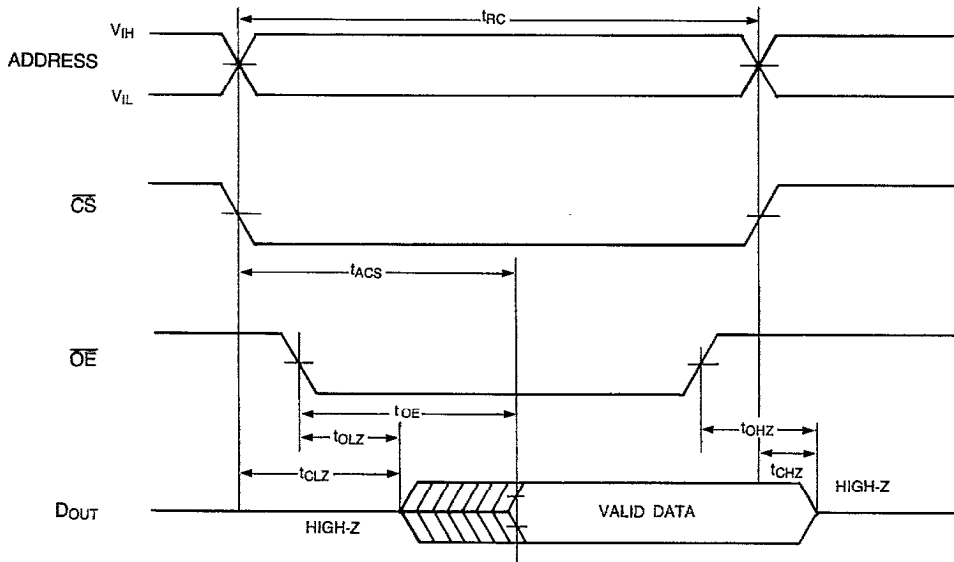
$C_L = 5\text{pF}$  (Includes Jig Capacitance)

**TIMING WAVEFORMS**

Read Cycle 1 (Notes 1, 3)



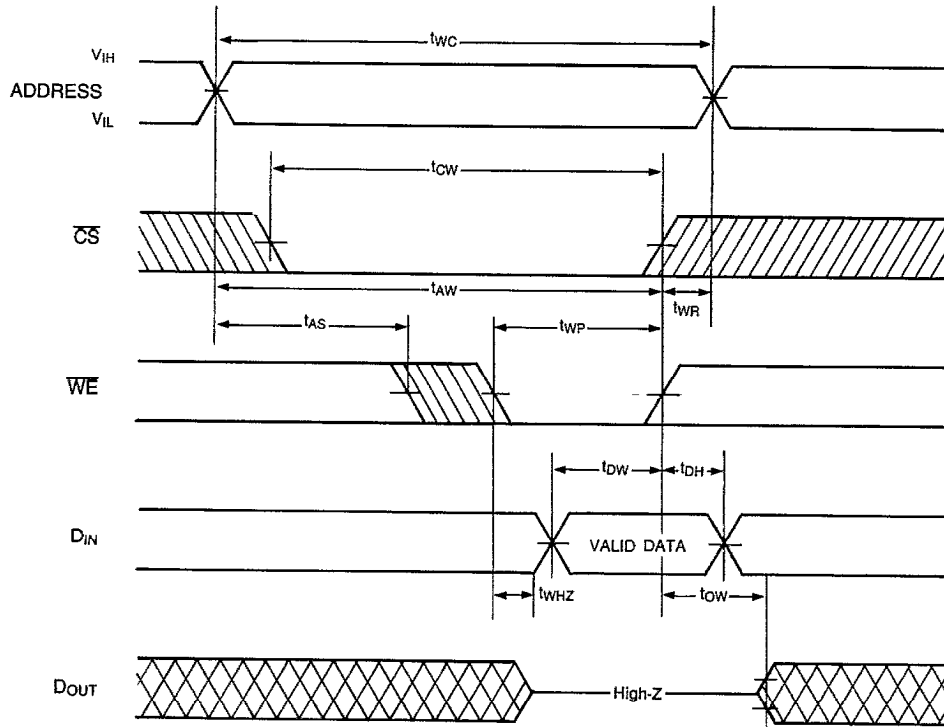
Read Cycle 2 (Notes 2, 3)



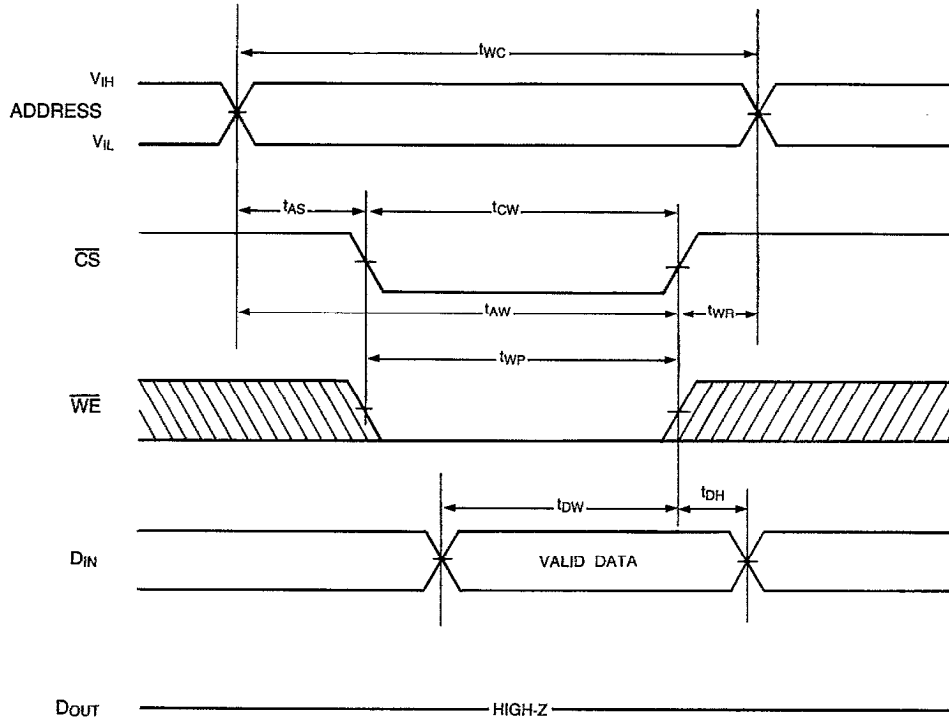
Notes:

1. Device is continuously selected.  $\overline{OE}, \overline{CS} = V_{IL}$
2. Address valid prior to or coincident with  $\overline{CS}$  transition low.
3.  $\overline{WE}$  is high for read cycle.

Write Cycle 1 ( $\overline{WE}$  Controlled) (Note 1, 2)



Write Cycle 2 ( $\overline{CS}$  Controlled) (Note 1, 2, 3)



Notes:

1. The internal write time of the memory is defined by the overlap of  $\overline{CS}$  low and  $\overline{WE}$  low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if  $\overline{OE} = V_{IH}$
3. If  $\overline{CS}$  goes high simultaneously with  $\overline{WE}$  high, the output remains in a high impedance state.

**Capacitance**

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1MHz V <sub>CC</sub> = 5.0V	—	6	pF
C <sub>OUT</sub>	Output Capacitance		—	8	

Note: Tested on a sample basis

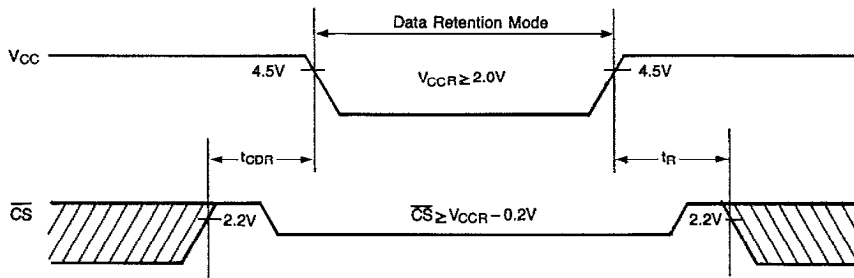
**Data Retention Characteristics: (T<sub>A</sub> = 0° ~ 70°C)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit	
V <sub>CCR</sub>	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	5.5	V	
I <sub>CCR</sub>	Data Retention Current	V <sub>CC</sub> = 3.0V CS ≥ 2.8V	AL	—	1**	50	μA
			ALL	—	0.5**	10	
t <sub>CDR</sub>	Chip Select Data Hold Time	Refer to the figure below	0	—	—	ns	
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> *	—	—	ns	

Note\* : Read Cycle Time

Note\*\*: Typ, Values are measured at 25°C.

**Data Retention Timing**



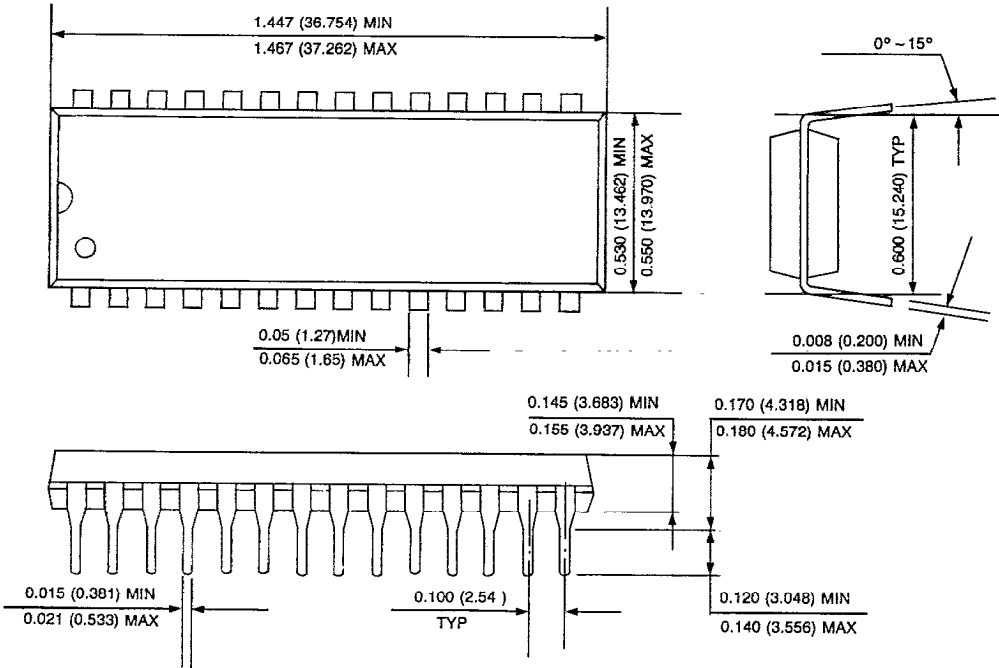
Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.



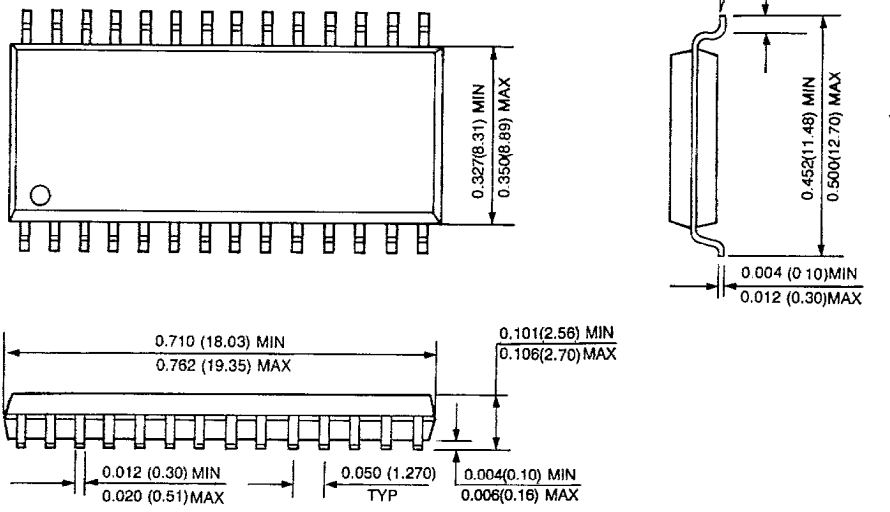
**Package Dimensions**

**28 DIP**

Unit: inches (mm)



**28 SOP**



28 TSOP

Unit: inches (mm)

