FUJITSU
MICROELECTRONICS, INC.

MB8264A

NMOS 65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB8264A-10
MB8264A-12
MB8264A-15

8264A-LCC

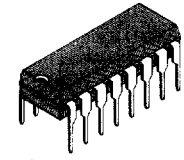
DESCRIPTION

The Fujitsu MB8264A is a fully decoded, dynamic NMOS random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

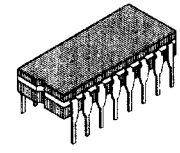
Multiplexed row and column address inputs permit the MB8264A to be housed in a standard 16-pin DIP and 18-pad LCC. With a JEDEC approved pin out.

The MB8264A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including dynamic sense amplifiers.

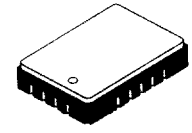
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs and the output are TTL compatible.



PLASTIC PACKAGE
DIP-16P-M03



CERDIP PACKAGE
DIP-16C-C04

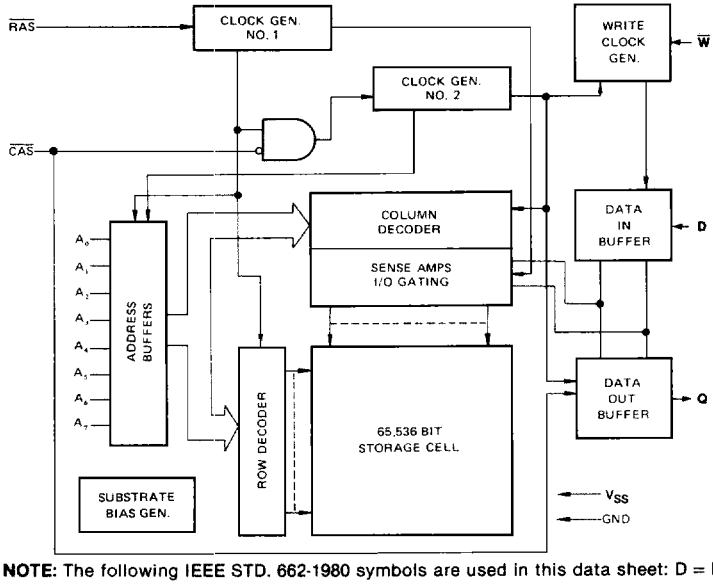


CERAMIC LCC
LCC-18C-F02

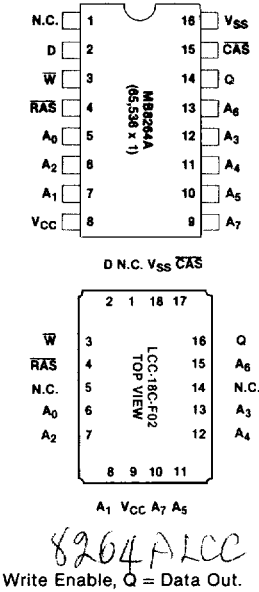
FEATURES

- **65,536 x 1-bit organization**
- **Row Access Time/Cycle Time**
  MB8264A-10 100 ns Max./200 ns Min.
  MB8264A-12 120 ns Max./230 ns Min
  MB8264A-15 150 ns Max./260 ns Min.
- **Low Max Power Dissipation (t_{RC} = min)**
  MB8264A-10 275 mW (Active)
  MB8264A-12 248 mW (Active)
  MB8264A-15 220 mW (Active)
  All devices 22 mW (Standby) max.
- **Single +5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **RAS only and hidden refresh**
- **2ms/128 cycle refresh**
- **Read-Modify-Write and Page Mode capability**
- **"Gated" $\overline{CAS}$**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Common I/O capability using "Early Write" operation**
- **On-chip Address and Data-in latches**
- **On-chip substrate bias generator**
- **t_{AR}, t_{WCR}, t_{DHR} eliminated**

MB8264A BLOCK DIAGRAM



PIN ASSIGNMENT



8264A-LCC

NOTE: The following IEEE STD. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

ABSOLUTE MAXIMUM RATINGS (See Note)

R7

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7.0	V
Storage Temperature	Cerdip	T_{stg}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

R4

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all Inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all Inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

R3

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance A_0 ~ A_7, D	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	—	8	pF
Output Capacitance Q	C_{OUT}	—	—	7	pF

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

R8

Parameter	Symbol	MB8264A-10		MB8264A-12		MB8264A-15		Unit
		Min	Max	Min	Max	Min	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	50	—	45	—	40	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}$/$\overline{CAS}$ = V_{IH})	I_{CC2}	—	4	—	4	—	4	mA
REFRESH CURRENT* Average Power Supply Current ($\overline{CAS}$ = V_{IH}; $\overline{RAS}$ cycling, t_{RC} = min.)	I_{CC3}	—	38	—	35	—	31	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}	—	35	—	32	—	28	mA
INPUT LEAKAGE CURRENT, any input (0V ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4	—	2.4	—	2.4	—	V
OUTPUT LEVEL, Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

R34

Parameter	Notes	Symbol		MB8264A-10		MB8264A-12		MB8264A-15		Unit
		Alternate	*Standard	Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	230	—	265	—	280	—	ns
Page Mode Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	135		155		180		ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	TCEHCEL	25	—	30	—	30	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	TCEHREL	0	—	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Reference to $\overline{CAS}$	(9)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(9)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Write Command Set Up Time	(8)	t_{WCS}	TWLCEL	0	—	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	35	—	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	35	—	40	—	45	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	40	—	50	—	60	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	(8)	t_{RWD}	TRELWL	90	—	110	—	120	—	ns

See notes on following page.

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor memory.

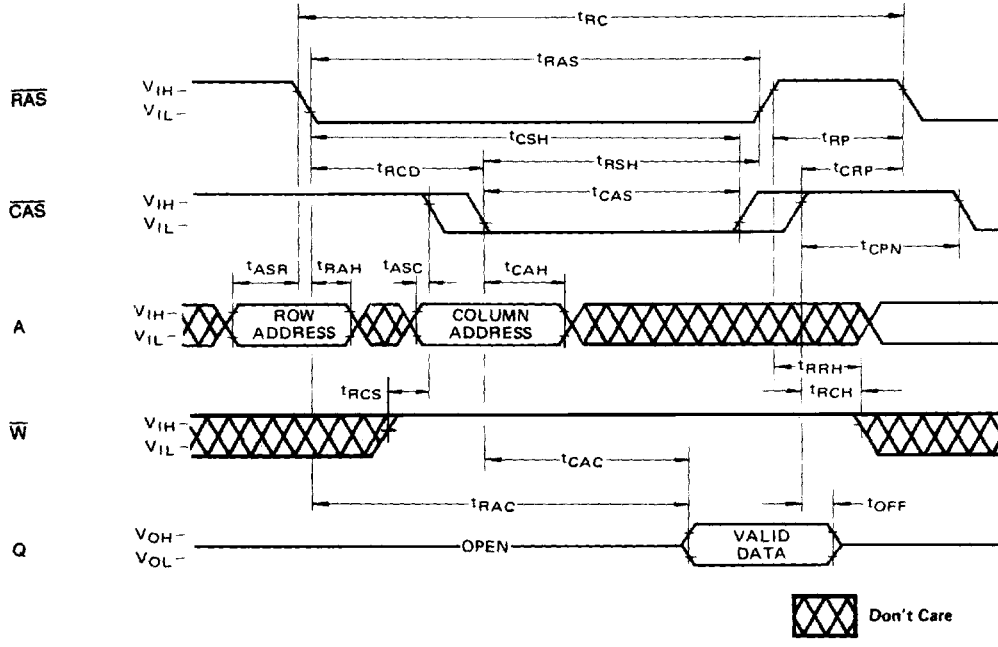
Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.); t_T = 5ns.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (high impedance) throughout entire cycle.

   If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

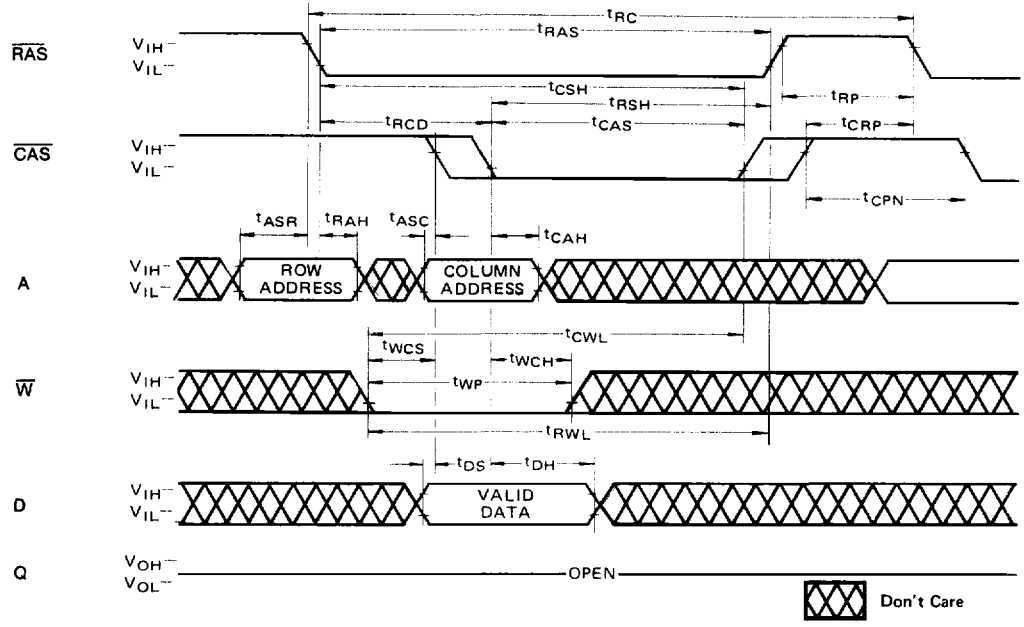
TIMING DIAGRAMS

READ CYCLE

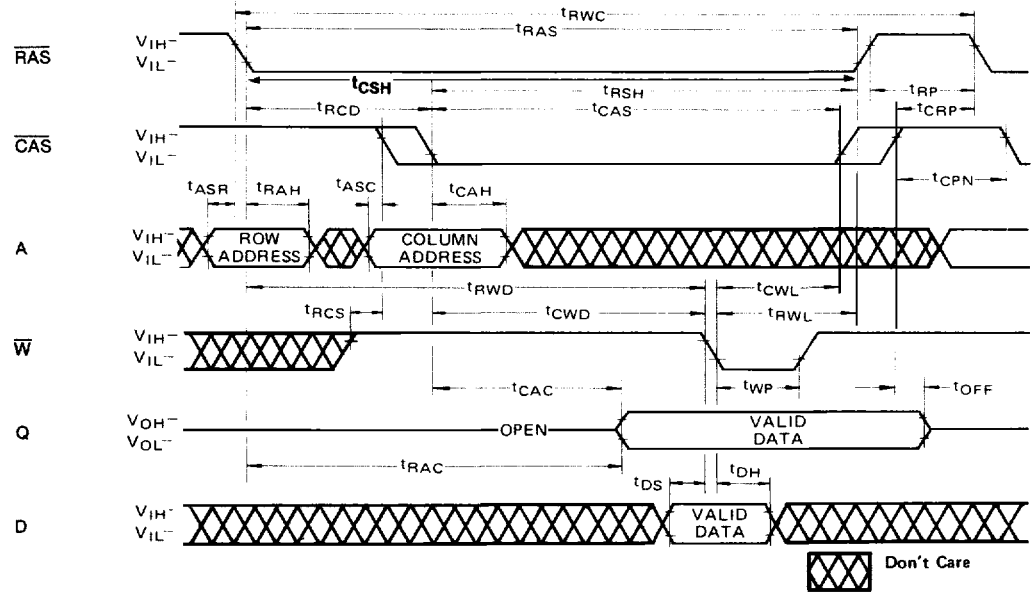


TIMING DIAGRAMS (Continued)

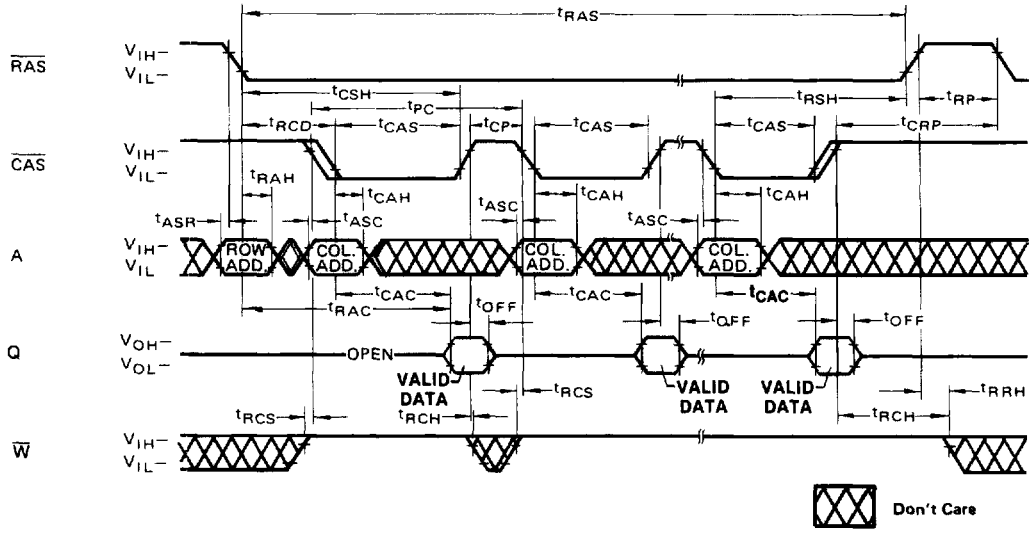
WRITE CYCLE (EARLY WRITE)



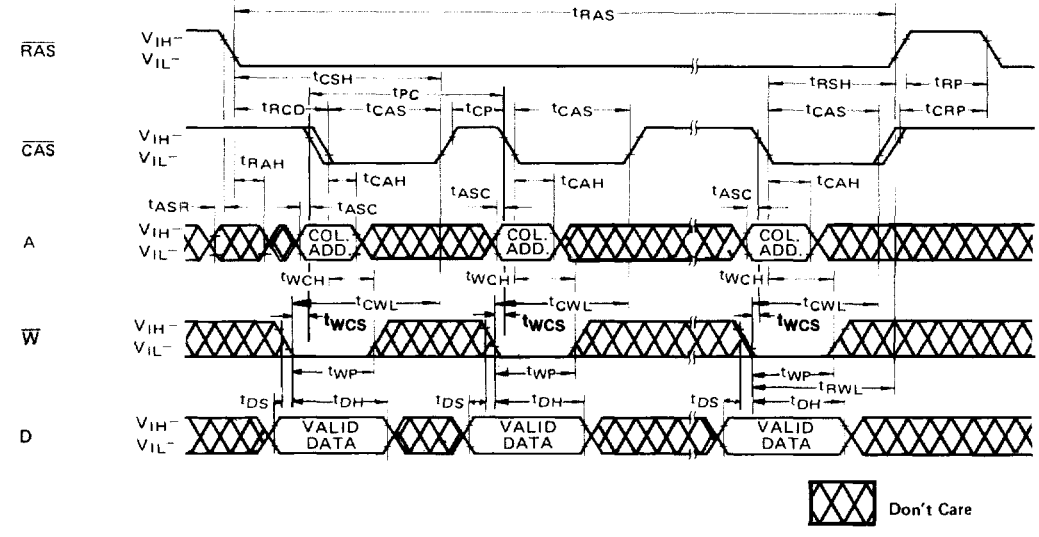
READ-WRITE/READ-MODIFY-WRITE CYCLE



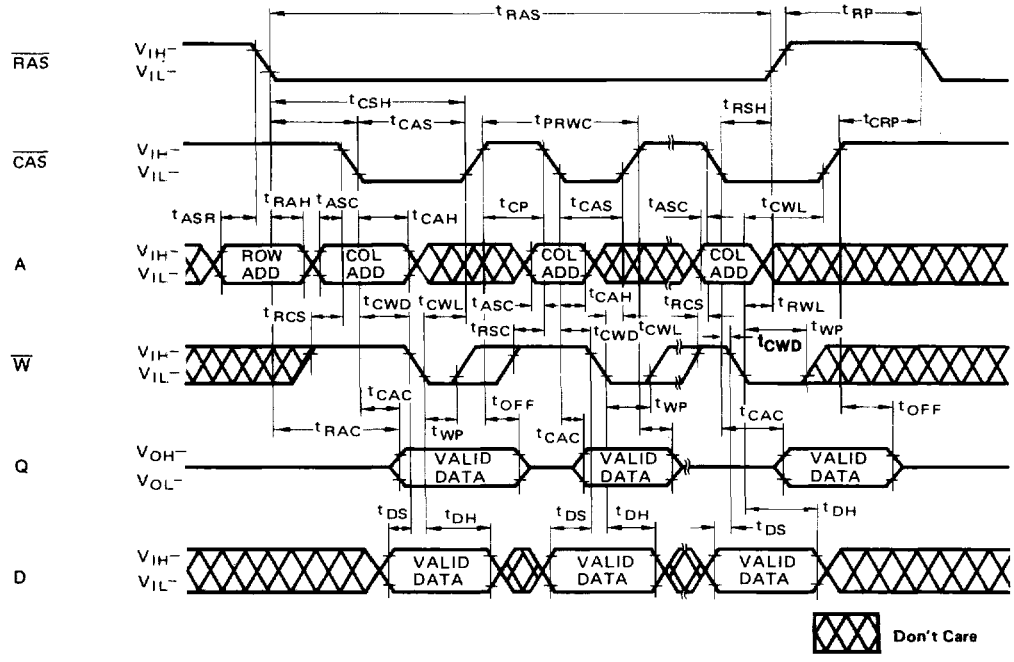
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

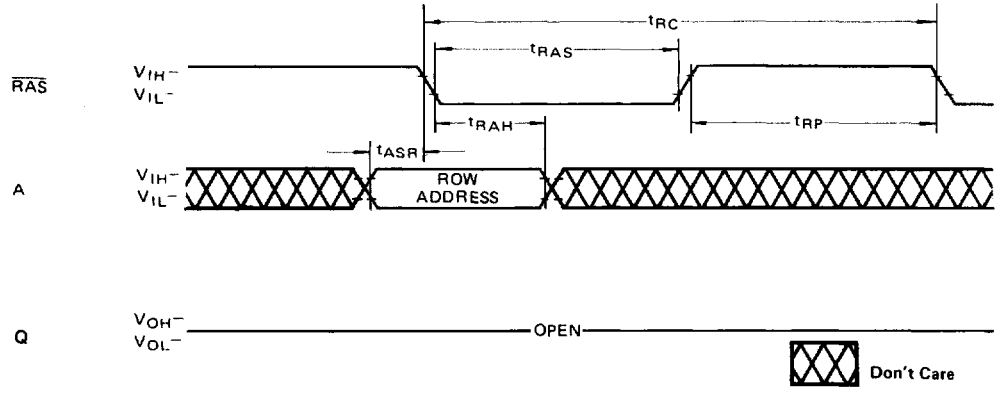


PAGE MODE READ-WRITE CYCLE

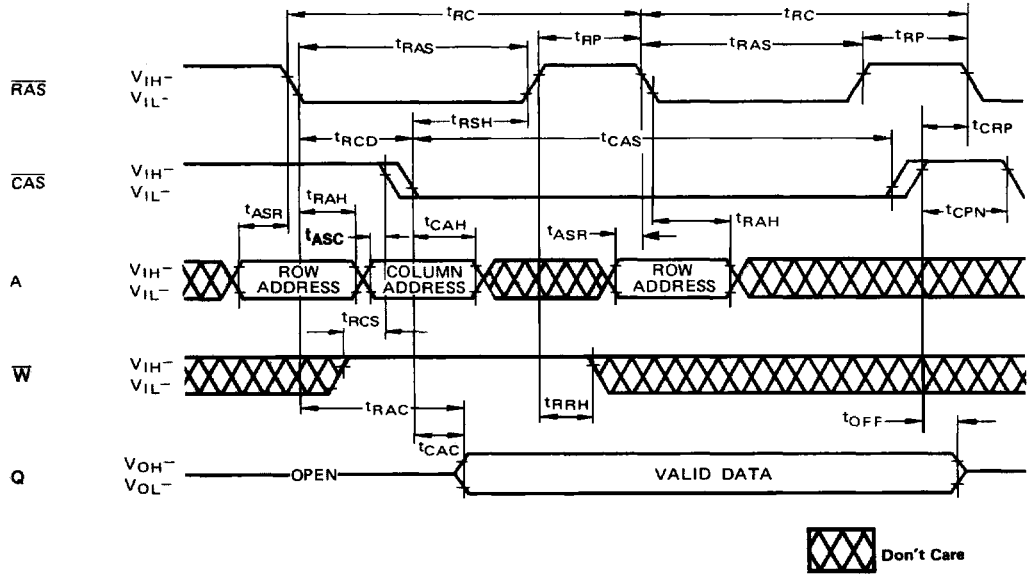


$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE



DESCRIPTION

Address Inputs

A total of sixteen binary input address bits are required to decode any one of 65,536 storage cell locations within the MB8264A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high (1) on $\overline{W}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264A during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (D) register. In a write cycle, if $\overline{W}$ is brought low (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8264A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

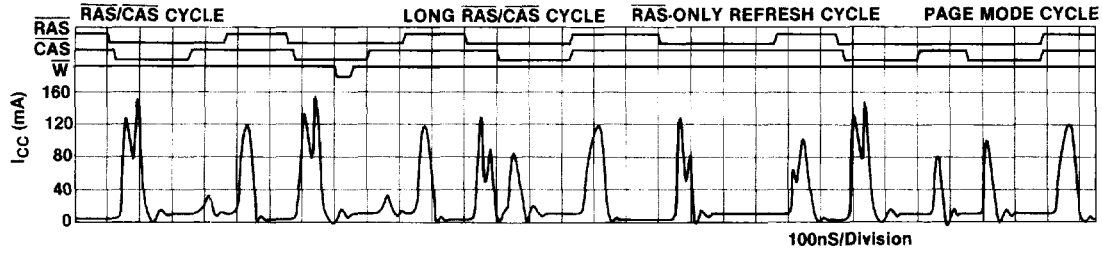
$\overline{RAS}$ Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0 ~ A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

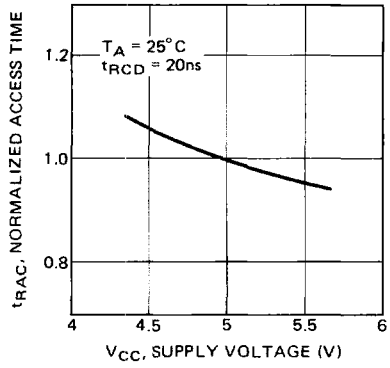
A $\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

CURRENT WAVEFORM (V_{CC} = 5.5V, TA = 25 °C)

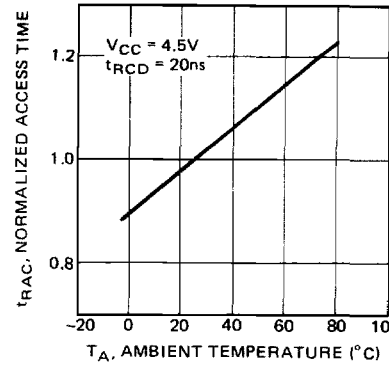


TYPICAL CHARACTERISTICS CURVES

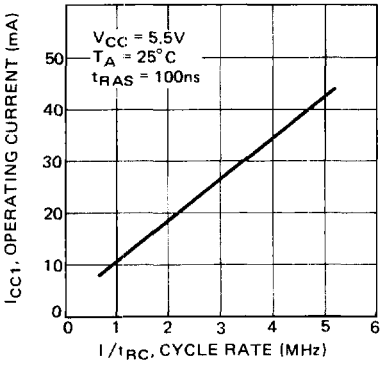
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



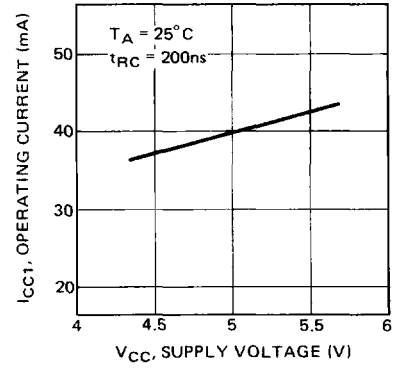
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



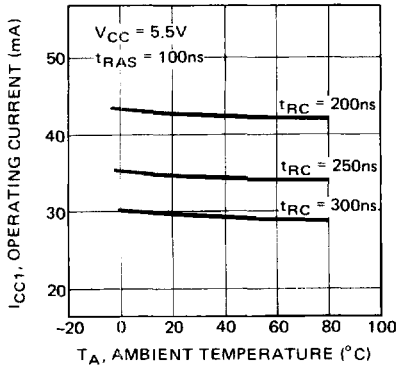
OPERATING CURRENT vs CYCLE RATE



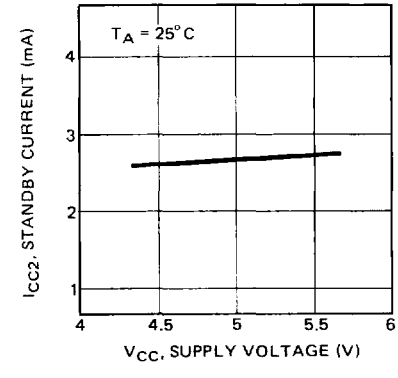
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

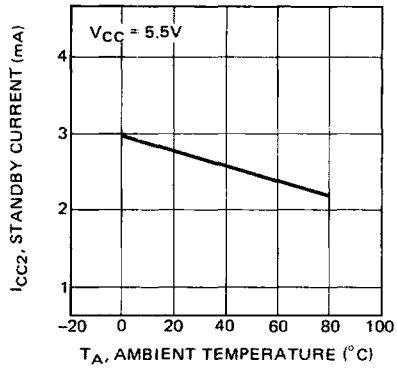


STANDBY CURRENT vs SUPPLY VOLTAGE

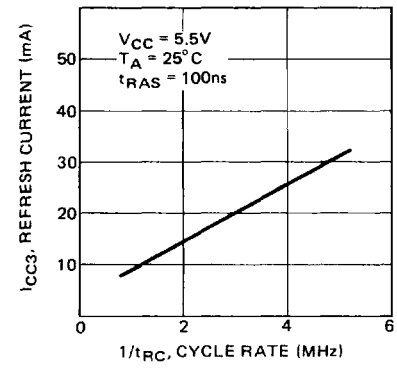


TYPICAL CHARACTERISTICS CURVES (Continued)

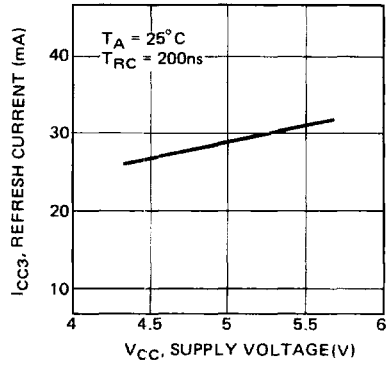
STANDBY CURRENT vs AMBIENT TEMPERATURE



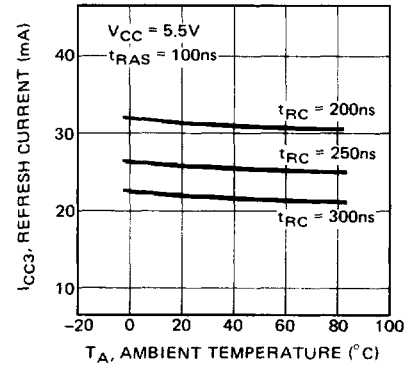
REFRESH CURRENT vs CYCLE RATE



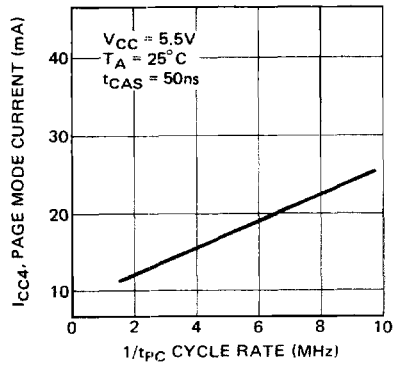
REFRESH CURRENT vs SUPPLY VOLTAGE



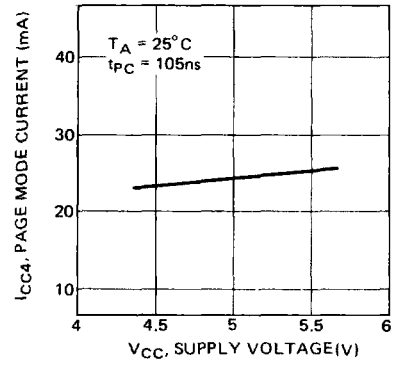
REFRESH CURRENT vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

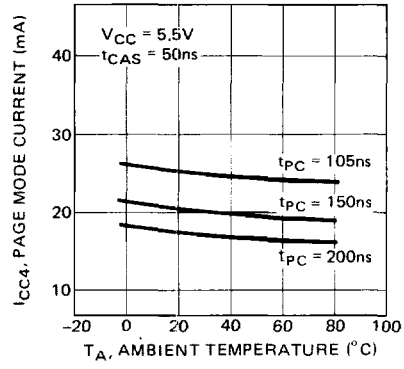


PAGE MODE CURRENT vs SUPPLY VOLTAGE

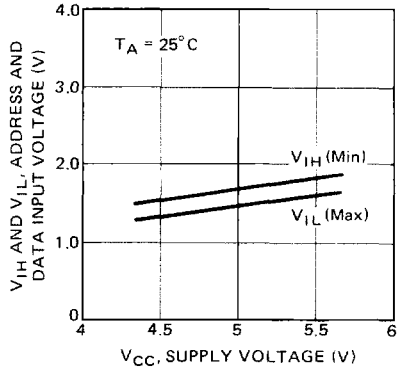


TYPICAL CHARACTERISTICS CURVES (Continued)

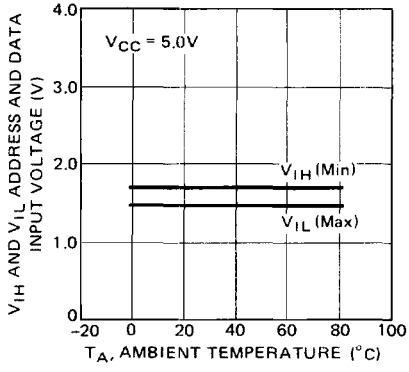
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



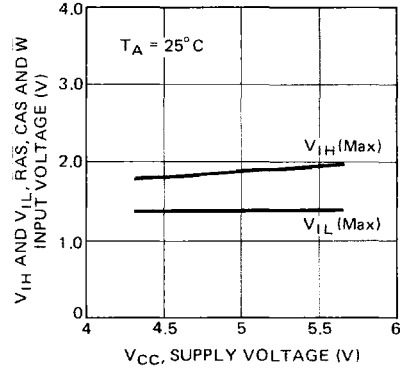
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE



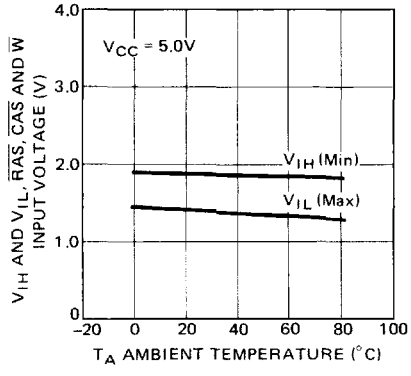
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

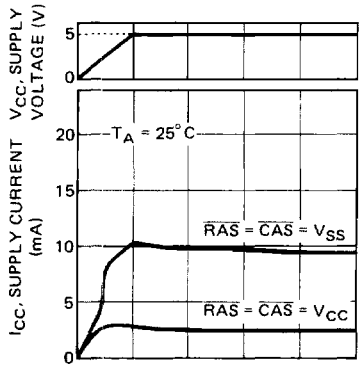


$\overline{RAS}$, $\overline{CAS}$ AND $\overline{W}$ VOLTAGE vs AMBIENT TEMPERATURE

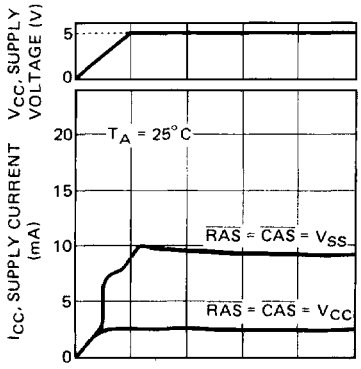


TYPICAL CHARACTERISTICS CURVES (Continued)

CURRENT WAVEFORM DURING POWER UP

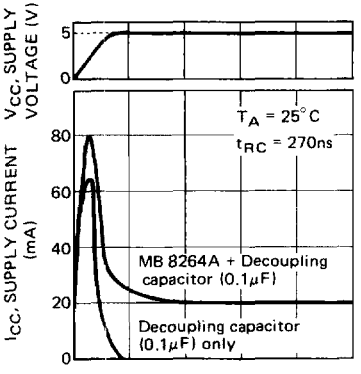


10μs/Division

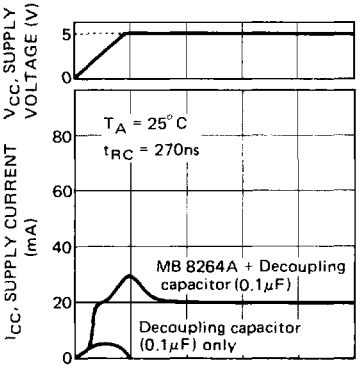


100μs/Division

CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)

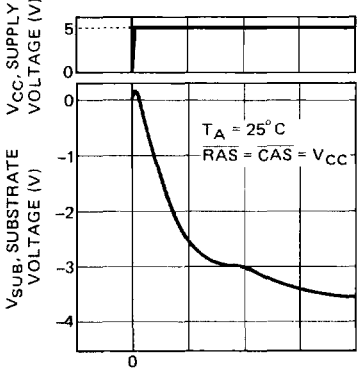


20μs/Division



100μs/Division

SUBSTRATE VOLTAGE vs SUPPLY VOLTAGE (DURING POWER UP)



50μs/Division