

## MCM2147

## **Advance Information**

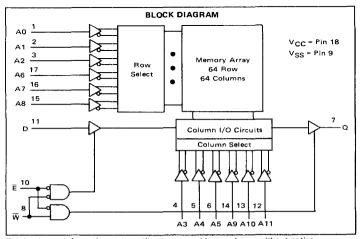
### 4096-BIT STATIC BANDOM ACCESS MEMORY

The MCM2147 is a 4096-bit static random access memory organized as 4096 words by 1-bit using Motorola's N-channel silicongate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

 $\overline{E}$  controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after  $\overline{E}$  goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as  $\overline{E}$  remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2147 is in an 18 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Fully Static Memory No Clock or Timing Strobe Required
- Single +5 V Supply
- High Density 18 Pin Package
- Automatic Power-Down
- Directly TTL Compatible—All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time MCM2147-55 = 55 ns max
   MCM2147-70 = 70 ns max
   MCM2147-85 = 85 ns max
   MCM2147-100 = 100 ns max



This is advance information and specifications are subject to change without notice.

## MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
also available



P SUFFIX PLASTIC PACKAGE CASE 707

### PIN ASSIGNMENT

AO	1	4.	18	VCC
A1	2	ď	17	A6
A2	3	d	16	A7
A3	4	d	15	A8
A4	5	d	14	A9
A5	6	d	13	A10
Q	7	d	12	A11
₩	8	d	11	D
V <sub>SS</sub>	9	d	10	Ê

### PIN NAMES

A0~A11	Address Input
w	Write Enable
Ē	Chip Enable
D	Data Input
Q	Data Output
Vcc	Power (+5 V)
V <sub>SS</sub>	Ground

### TRUTH TABLE

Ē	W	Mode	Output	Power
Н	×	Not Selected	High Z	Standby
L	L.	Write	High Z	Active
ī	н	Read	Data Out	Active

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ADI-479 R1

### ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Value	Unit
Temperature Under Bias	-10 to +85	°С
Voltage on Any Pin With Respect to VCC	-0.5 to +7.0	Vdc
DC Output Current	20	mA
Power Dissipation	1.0	Watt
Operating Temperature Range	0 to +70	°c
Storage Temperature Range	-65 to +150	°c

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

### DC OPERATING CONDITIONS AND CHARACTERISTICS (TA = 0 to 70°C, V<sub>CC</sub> = 5.0 V ± 5% unless otherwise noted.)

		MCM2147-55 MCM 2147-70				MC	M2147	-85	MCN					
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Load Current (All Input Pins, V <sub>in</sub> = 0 to 5.5 V)	<sup>1</sup> IL.	-	0.01	10	-	0.01	10	_	0.01	10	-	0.01	10	μА
Output Leakage Current (E = 2.0 V, V <sub>out</sub> = 0 to 5.5 V)	lor	-	0.1	50	-	0.1	50	_	0.1	50	-	0.1	50	μΑ
Power Supply Current (E = V <sub>IL</sub> , Outputs Open, T <sub>A</sub> = 25 <sup>o</sup> C)	ICC1	_	120	170	-	100	150		95	130	_	90	110	mA
Power Supply Current (E = V <sub>IL</sub> , Outputs Open, T <sub>A</sub> = 0 <sup>o</sup> C)	<sup>1</sup> CC2	-		180	-	-	160	-	-	140	-	1	120	mA
Standby Current (E = V <sub>IH</sub> )	I <sub>SB</sub>	-	15	30	-	10	20	-	15	25	-	10	20	mA
Input Low Voltage	VIL	-0.3		8.0	-0.3	_	0.8	-0.3	-	8.0	-0.3	_	8.0	V
Input High Voltage	VIH	2.0		6.0	2.0	-	6.0	2.0	_	6.0	2.0	-	6.0	V
Output Low Voltage (IOL = 8.0 mA)	VOL	-		0.4	_	_	0.4	_		0.4	-	_	0.4	٧
Output High Voltage (I <sub>OH</sub> = -4.0 mA)	∨он	2.4		_	2.4	_	_	2.4			2.4	_		V

Typical values are for  $T_A = 25^{\circ}C$  and  $V_{CC} = +5.0 \text{ V}$ .

### CAPACITANCE

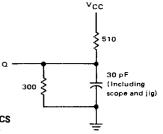
(f = 1.0 MHz,  $T_A$  = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (Vin = 0 V)	Cin	5.0	ρF
Output Capacitance (Vout = 0 V)	Cout	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated

from the equation:  $C = \frac{I\Delta_t}{\Delta V}$ .

## FIGURE 1 — OUTPUT LOAD



### **AC OPERATING CONDITIONS AND CHARACTERISTICS**

(Full operating voltage and temperature unless otherwise noted.)

Input Pulse Levels	٠		٠	٠	٠	٠	•	•	•	•	٠.	•	٠	U	٧	O	ττο	3,5	Voits
Input Flise and Fall Times																			10 ns
Input and Output Timing Levels																		1.5	Volts
Output Load																	Se	e Fi	gure 1



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## AC OPERATING CONDITIONS AND CHARACTERISTICS, Read, Write Cycles (TA = 0 to 70°C, VCC = 5.0 V ± 5%)

		мсм2	147-55	MCM2147~70		MCM2	147-85	47-85 MCM2147-100		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Address Valid to Address Don't Care (Cycle Time When Chip Enable is Held Active)	tAVAX	55	-	70	-	85	_	100	_	ns
Chip Enable Low to Chip Enable High	†AVQV		55	_	70		85		100	ns
Address Valid to Output Valid (Access)	tELQV1*	<u> </u>	55		70		85	_	100	ns
Chip Enable Low to Output Valid (Access)	tELQV2*	_	65	-	80		95	_	110	ns
Address Valid to Output Invalid	tAVQX	10	_	10	_	10	_	10		ns
Chip Enable Low to Output Invalid	†ELQX	10	_	10		10		10	_	ns
Chip Enable High to Output High Z	<sup>t</sup> EHQZ	0	40	0	40	0	40	0	40	ns
Chip Selection to Power-Up Time	tpU	0	l – .	0		0	-	0	_	ns
Chip Deselection to Power-Down Time	tPD	0	30	0	30	0	30	0	30	ns
Address Valid to Chip Enable Low (Address Setup)	tAXEL	0		0		0	_	0	_	ns
Chip Enable Low to Write High	tELWH	45		55		70		80		ns
Address Valid to Write High	tAVWH	45		55	_	70		80		пѕ
Address Valid to Write Low (Address Setup)	tAVWL	0	_	0		0	-	0	-	nş
Write Low to Write High (Write Pulse Width)	tWLWH	35	_	40		55		65		ns
Write High to Address Don't Care	tWHAX	10		15		15	Γ	15	_	ns
Data Valid to Write High	¹DVWH	25		30		45		55		ns
Write High to Data Don't Care (Data Hold)	twHDX	10	T -	10		10	_	10		ns
Write Low to Output High Z	tWLQZ	0	30	0	35	0	45	0	50	ns
Write High to Output Valid	twhqv	0	<u> </u>	0		0	L <u>-</u> _	0		ns

<sup>\*</sup>telQV1 is access from chip enable when the 2147 is deselected for at least 55 ns prior to this cycle, telQV2 is access from chip enable for 0 ns < deselect time < 55 ns. If deselect time = 0 ns, then telQV = tavQV.

## TIMING PARAMETER ABBREVIATIONS

signal name from which interval is defined — transition direction for first signal signal name to which interval is defined transition direction for second signal

The transition definitions used in this data sheet are:

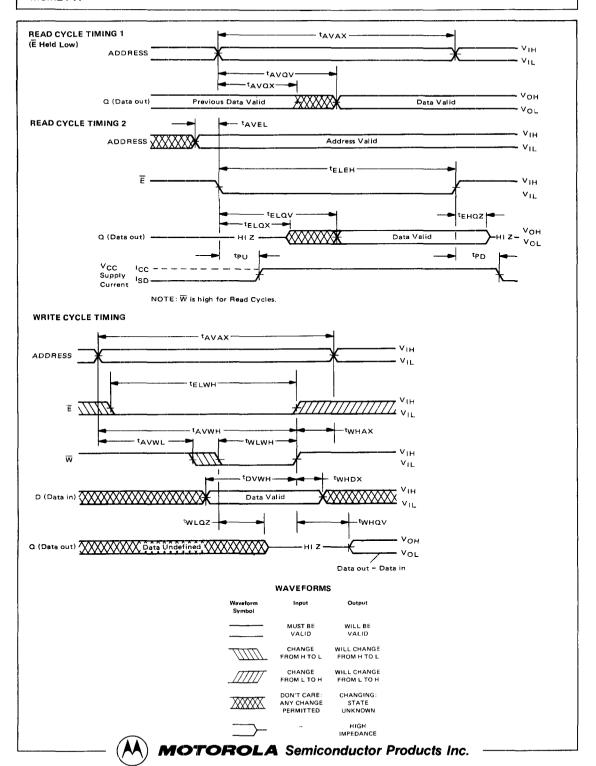
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

## TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.



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### DEVICE DESCRIPTION

The MCM2147 is produced with a high-performance MOS technology which combines on-chip substrate bias generation with device scaling to achieve high speed. The speed-power product of this process is about four times better than earlier MOS processes.

This gives the MCM2147 its high speed, low power and ease-of-use. The low-power standby feature is controlled with the  $\overline{E}$  input.  $\overline{E}$  is not a clock and does not have to be cycled. This allows the user to tie  $\overline{E}$  directly to system addresses and use the line as part of the normal decoding logic. Whenever the MCM2147 is deselected, it automatically reduces its power requirements.

### SYSTEM POWER SAVINGS

The automatic power-down feature adds up to significant system power savings. Unselected devices draw low standby power and only the active devices draw active power. Thus the average power consumed by a device declines as the system size increases, asymptotically approaching the standby power level as shown in Figure 2.

The automatic power-down feature is obtained without any performance degradation, since access time from chip enable is ≤ access time from address valid. Also the fully static design gives access time equal cycle time so multiple read or write operations are possible during a single select period. The resultant data rates are 14.3 MHz and 18 MHz for the MCM2147-70 and MCM2147-55 respectively.

# DECOUPLING AND BOARD LAYOUT CONSIDERATIONS

The power switching characteristic of the MCM2147 requires careful decoupling. It is recommended that a 0.1  $\mu$ F to 0.3  $\mu$ F ceramic capacitor be used on every other device, with a 22  $\mu$ F to 47  $\mu$ F bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle.

Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 3. If fast drivers are used, terminations are recommended on input signal lines to the MCM2147 because significant reflections are possible when driving their high impedance inputs. Terminations may be required to match the impedance of the line to the driver.

FIGURE 2 — AVERAGE DEVICE DISSIPATION
VERSUS MEMORY SIZE

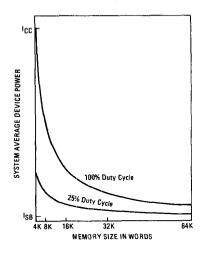
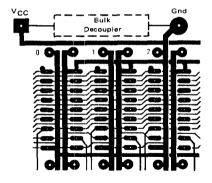


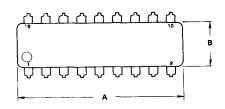
FIGURE 3 - PC LAYOUT

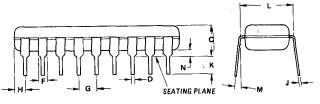




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## PACKAGE DIMENSIONS





	MILLIN	METERS	INC	HES				
DIM	MIN	MIN MAX. MIN						
Α	22.22	23.24	0.875	0.915				
В	6.60	7.11	0.260	0.280				
C	4.06	4.57	0.160	0.180				
D	0.36	0.51	0.014	0.020				
F	1.02	1.52	0.040	0.060				
G	2.41	2.67	0.095	0.105				
Н	1.14	1.40	0.045	0.055				
J	0.20	0.30	0.008	0.012				
K	3.05	3.56	0.120	0.140				
L	7.37	7.87	0.290	0.310				
М	.00	10°	00	10 <sup>0</sup>				
N	0.51	1.02	0.020	0.040				

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