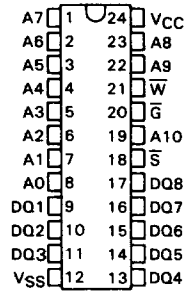
TMS4016
2048-WORD BY 8-BIT STATIC RAM

FEBRUARY 1981 – REVISED AUGUST 1983

- 2K X 8 Organization, Common I/O
- Single +5-V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600 Mil (15.2 mm) Package Configuration
- Plug-in Compatible with 16K 5 V EPROMs
- 8-Bit Output for Use in Microprocessor-Based Systems
- 3-State Outputs with $\overline{S}$ for OR-ties
- $\overline{G}$ Eliminates Need for External Bus Buffers
- All Inputs and Outputs Fully TTL Compatible
- Fanout to Series 74, Series 74S or Series 74LS TTL Loads
- N-Channel Silicon-Gate Technology
- Power Dissipation Under 385 mW Max
- Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads
- 4 Performance Ranges:

	ACCESS TIME (MAX)
TMS4016-12	120 ns
TMS4016-15	150 ns
TMS4016-20	200 ns
TMS4016-25	250 ns

TMS4016 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4016 static random-access memory is organized as 2048 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS4016 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS4016 static RAM has the same standardized pinout as TI's compatible EPROM family. This, along with other compatible features, makes the TMS4016 plug-in compatible with the TMS2516 (or other 16K 5 V EPROMs). Minimal, if any modifications are needed. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

The TMS4016 is offered in the plastic (NL suffix) 24-pin dual-in-line package designed for insertion in mounting hole rows on 600-mil (15.2 mm) centers. It is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0 – A10)

The eleven address inputs select one of the 2048 8-bit words in the RAM. The address-inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

output enable ($\overline{G}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in/data-out terminals. When chip select and output enable are at a logic low level, the D/Q terminals are enabled. When chip select is high, the D/Q terminals are in the floating or high-impedance state and the input is inhibited.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1 – DQ8)

Data can be written into a selected device when the write enable input is low. The D/Q terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate, one Series 74S TTL gate, or five Series 74LS TTL gates. The D/Q terminals are in the high impedance state when chip select ($\overline{S}$) is high, output enable ($\overline{G}$) is high, or whenever a write operation is being performed. Data-out is the same polarity as data-in.

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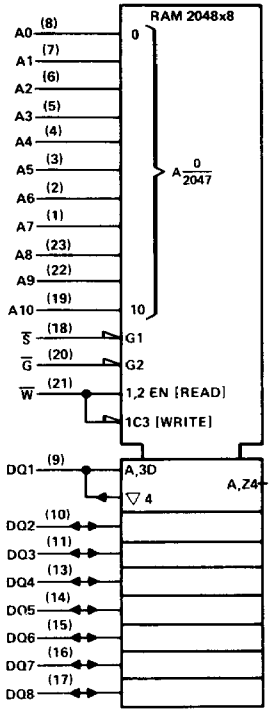
logic symbol†



FUNCTION TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	DQ1-DQ8	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage (any input) (see Note 1) . . . . . −1 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the V_{SS} terminal.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High level voltage	$I_{OH} = -1$ mA,	$V_{CC} = 4.5$ V	2.4			V
V_{OL}	Low level voltage	$I_{OL} = 2.1$ mA,	$V_{CC} = 4.5$ V			0.4	V
I_I	Input current	$V_I = 0$ V to 5.5 V				10	μA
I_{OZ}	Off-state output current	$\overline{S}$ or $\overline{G}$ at 2 V or $\overline{W}$ at 0.8 V, $V_O = 0$ V to 5.5 V				10	μA
I_{CC}	Supply current from V_{CC}	$I_O = 0$ mA, $T_A = 0°C$ (worst case)	$V_{CC} = 5.5$ V,		40	70	mA
C_i	Input capacitance	$V_I = 0$ V,	$f = 1$ MHz			8	pF
C_o	Output capacitance	$V_O = 0$ V,	$f = 1$ MHz			12	pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS4016-12		TMS4016-15		TMS4016-20		TMS4016-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	120		150		200		250		ns
$t_{c(wr)}$	Write cycle time	120		150		200		250		ns
$t_{w(W)}$	Write pulse width	60		80		100		120		ns
$t_{su(A)}$	Address setup time	20		20		20		20		ns
$t_{su(S)}$	Chip select setup time	60		80		100		120		ns
$t_{su(D)}$	Data setup time	50		60		80		100		ns
$t_{h(A)}$	Address hold time	0		0		0		0		ns
$t_{h(D)}$	Data hold time	5		10		10		10		ns

switching characteristics over recommended voltage range, $T_A = 0°C$ to $70°C$ with output loading of Figure 1 (see notes 3 and 4)

PARAMETER		TMS4016-12		TMS4016-15		TMS4016-20		TMS4016-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		120		150		200		250	ns
$t_{a(S)}$	Access time from chip select low		60		75		100		120	ns
$t_{a(G)}$	Access time from output enable low		50		60		80		100	ns
$t_{v(A)}$	Output data valid after address change	10		15		15		15		ns
$t_{dis(S)}$	Output disable time after chip select high		40		50		60		80	ns
$t_{dis(G)}$	Output disable time after output enable high		40		50		60		80	ns
$t_{dis(W)}$	Output disable time after write enable low		50		60		60		80	ns
$t_{en(S)}$	Output enable time after chip select low	5		5		10		10		ns
$t_{en(G)}$	Output enable time after output enable low	5		5		10		10		ns
$t_{en(W)}$	Output enable time after write enable high	5		5		10		10		ns

NOTES: 3. $C_L = 100$ pF for all measurements except $t_{dis(W)}$ and $t_{en(W)}$.
$C_L = 5$ pF for $t_{dis(W)}$ and $t_{en(W)}$.
4. t_{dis} and t_{en} parameters are sampled and not 100% tested.

PARAMETER MEASUREMENT INFORMATION

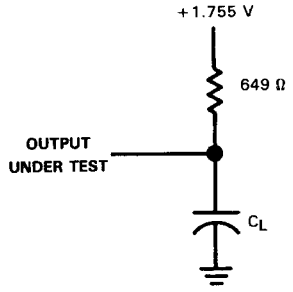
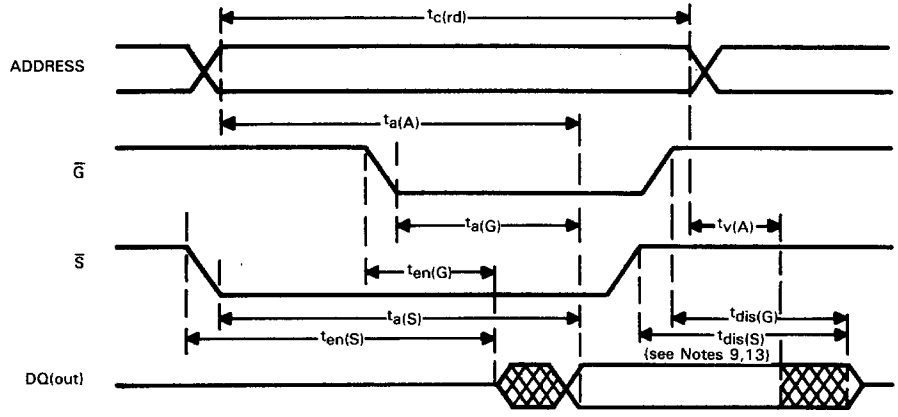


FIGURE 1 – OUTPUT LOAD

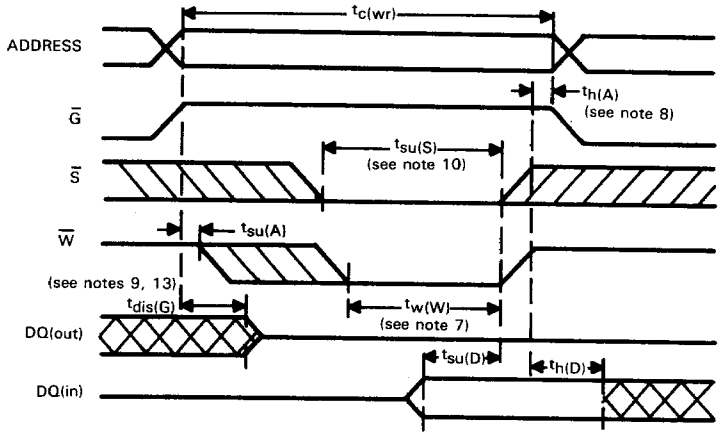
timing waveform of read cycle (see note 5)



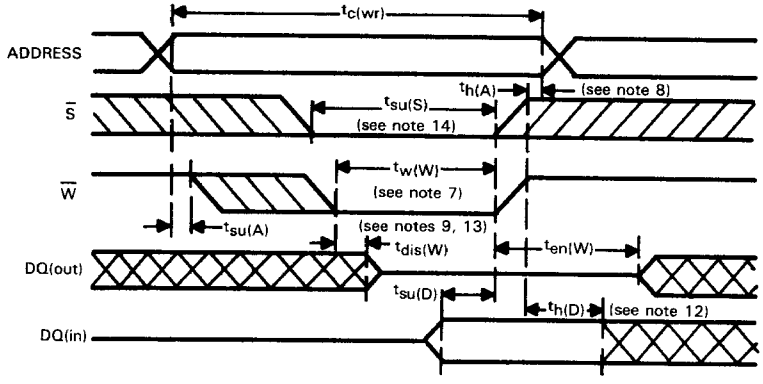
All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 ns.

NOTE 5: $\overline{W}$ is high for Read Cycle.

timing waveform of write cycle no. 1 (see note 6)



timing waveform of write cycle no. 2 (see notes 6 and 11)



All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

NOTES:
6. $\overline{W}$ must be high during all address transitions.
7. A write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
8. $t_{h(A)}$ is measured from the earlier of $\overline{S}$ or $\overline{W}$ going high to the end of the write cycle.
9. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
10. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, output remains in a high impedance state.
11. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
12. If $\overline{S}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
13. Transition is measured ±200 mV from steady-state voltage.
14. If the $\overline{S}$ low transition occurs before the $\overline{W}$ low transition, then the data input signals of opposite phase to the outputs must not be applied for the duration of $t_{dis(W)}$ after the $\overline{W}$ low transition.